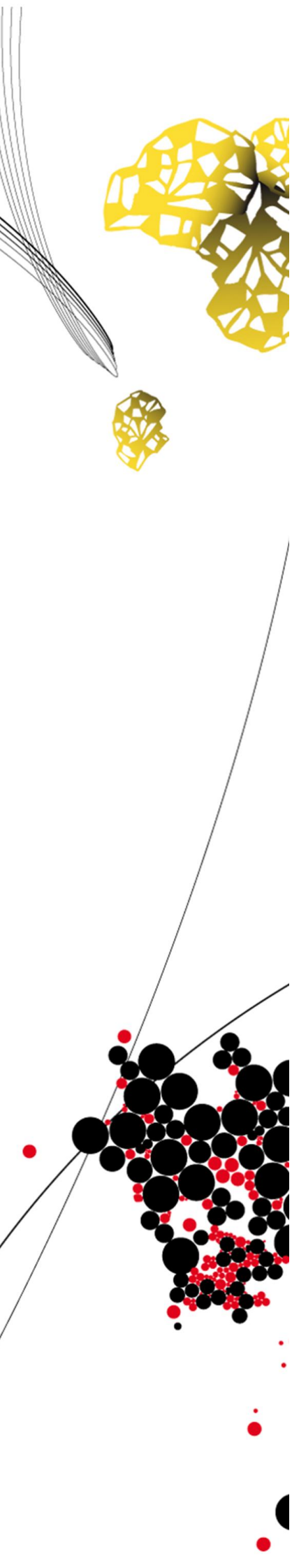

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High $IMFDR_3$ Switched-Capacitor Amplifier design in CMOS 65nm

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Abstract:

Due to the continuous feature size downscaling trend of integrated circuit (IC) technologies and their corresponding supply voltages realizing high dynamic range (DR) receiver (RX) front-ends becomes increasingly problematic. Therefore a new 'mixer-first' receiver front-end is envisioned, in which the mixer (MIX) is directly connected to the antenna, instead of using a traditional receiver front-end, in which the mixer is preceded with a low noise amplifier (LNA) stage limiting the dynamic range. A proper subsequent amplifier (AMP) stage is however still lacking being the focus in this document. Since the mixer stage already limits the noise performance the initial focus is upon realizing a highly linear amplifier.

Knowing the initial desire to design a highly linear amplifier an amplifier topology is proposed, the dominant distortion mechanism determined and an optimization for high linearity suggested. Regarding the noise also the dominant contributing mechanism and an optimization method are revealed. Both parameters are considered for complementary metal-oxide–semiconductor (CMOS) 65nm integrated circuit technology being the current design technology node.

Regarding the already existing literature, uniqueness is found in applying capacitive- rather than resistive feedback, with high linearity as the dominant design consideration. Also the switched biasing inside the capacitive feedback network is uncommon, allowing different Op Amp input- and output common-mode (CM) voltages. Finally the majority of the research already available is for old integrated circuit technologies and this document may hence provide additional insights for upcoming technology design nodes.

The obtained amplifier performance specifications are an input-referred third-order intercept point (IIP_3) of 19.6dBm. An equivalent input-referred noise voltage (EIRNV) of 2.93nV/√Hz (at 20MHz). A closed-loop (CL) gain (A_{CL}) and bandwidth (BW_{CL}) of 11.9dB respectively 88.5MHz with a power consumption of 11.2mW.

Contents:

1 Introduction:

This introduction chapter starts by giving a project description {1.1}. Knowing the context of the project will enable one to focus upon the literature that should be read. Important results from the literature reviewed are stated in {1.2}. With this additional knowledge shortcommings became evident regarding project realization. These shortcomings served as a framework on which this report is written as can be read in {1.3}.

1.1 Project description:

1.1.1 Subject: Properties of the radio frequency (RF) environment, like the presence of strong interferers and large signal propagation losses [3], require high linearity and low noise radio front-ends [2]. Traditionally this required the concept radio front-end displayed in {Figure 1} below.

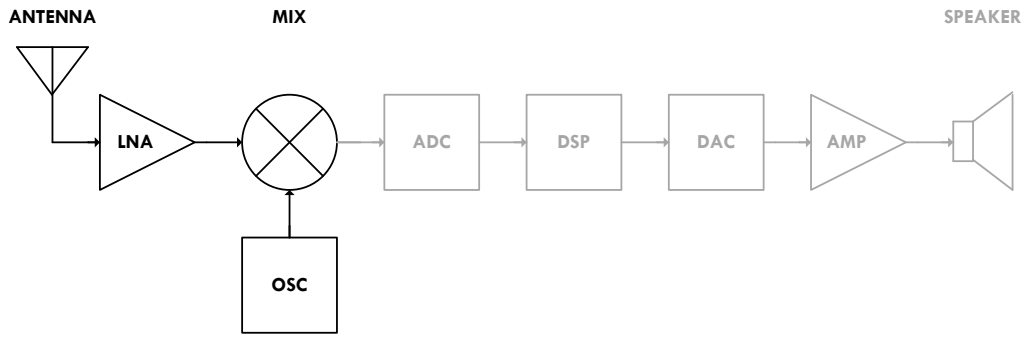

Figure 1: Traditional RX-architecture (radio front-end highlighted)

At the antenna the electromagnetical wave is converted into a power signal before being applied to the LNA. The LNA is applied to attenuate the generally large noise contribution from the subsequent receiver architecture stages but does this for it's linearity as well. (Friis theory of cascaded stages reveals that both the linearity and the noise are downscaled by the gain of preceding stages). The mixer is applied to downconvert the input signal frequency and for this is driven with an oscillator (OSC). Downconverting the input signal frequency from RF to intermediate frequencies (IF) makes signal processing easier, due to e.g. the larger gains available. In the digital domain a digital signal processor (DSP) is used to increase the robustness of the radio link with techniques as e.g. interleaving- and bit error correction upon the received data. The conversion between the analog- and digital domain is facilitated with an analog-to-digital converter (ADC) explaining the complete radio front-end setup in {Figure 1} above.

The LNA downscaling regarding the linearity and the noise of the subsequent receiver architecture lead to the idea to investigate a radio front-end without LNA as displayed in {Figure 2}. Where normally the mixer noise was kept low with the gain of the preceding LNA, this is now tried for with a Tayloe mixer [7] and making use of uncorrelated signal paths [8]. This however requires differential signalling and hence the use of baluns as indicated.

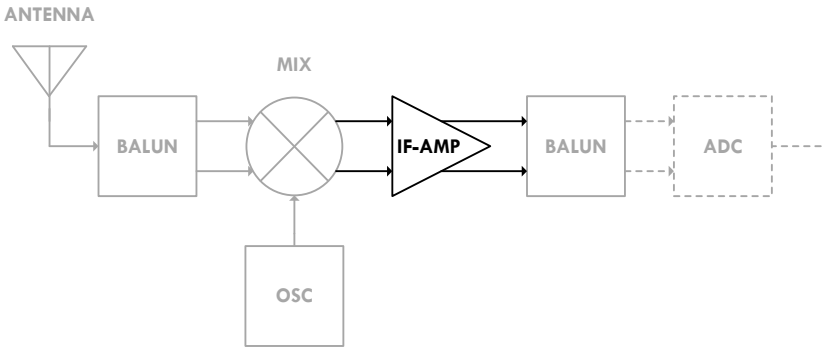

Figure 2: Envisioned RX-architecture (partly displayed) with IF-AMP highlighted

The gain previously facilitated by the LNA is now realized with an IF-AMP at the backside of the mixer. Hence the current research request to design a high linearity and low noise (high $IMFDR_3$ {1.2.1}) fully differential amplifier (FDA).

1.1.2 Specifications: The specifications to which the circuit should comply are listed below, in order of importance, with the most important one at the top.

1. Fully differential in standard CMOS 65nm 1.2V IC technology
2. $IIP_3 \geq 20dBm$
3. $EIRNV \leq 3nV/\sqrt{Hz}$
4. $A_{CL} \geq 4$
5. $BW_{CL} \geq 25MHz$
6. $Power \leq 10mW$
7. Input impedance = ‘High’

Fully differential: Differential signalling is a method of transmitting information by means of two complementary signals, as opposed to single ended signalling in which all the information is transmitted in a single signal. Differential signalling offers certain benefits not provided for by single ended signalling, like e.g. even-order distortion suppression and common-mode rejection. Recognizing distortion suppression as linearity improvement, this signalling method is applied. Clearly with differential signalling the amplifier requires two input- and output ports know as being a fully differential implementation.

Standard CMOS 65nm 1.2V IC technology: With different IC technologies available standard (digital) CMOS is known for offering relatively cheap manufacturing possibilities. Build from n-type- and p-type metal oxide semiconductor transistors (NMOST & PMOST) this technology provides low power consumption when driven by digital signals, lowering heat problems, and hence is optimized for digital circuits. With decreasing on chip feature sizes digital circuits can perform increasing more functionality on the same chip area meaning for constant costs. This explains the feature size downscaling trend with time arriving at the 65nm technology node nowadays. Trying to make advantage of the relatively cheap manufacturing possibility, analog circuits are integrated with the digital circuits on the same chip, explaining the standard CMOS 65nm integrated circuit technology design choice.

1.2 Literature review:

1.2.1 DR, SFDR, IMFDR and IMFDR$_3$: The dynamic range is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit provides a reasonable signal quality. Setting the upper end of the dynamic range on the intermodulation behaviour and the lower end on the sensitivity is called the spurious-free dynamic range (SFDR) [2]. The sensitivity in turn is defined as the minimum input signal level that still yields a minimum signal-to-noise ratio (SNRmin) at the output [2].

$$P_{IN,MIN} = F + SNR_{MIN} \tag{1.1}$$

F is the total integrated noise of the system, also called the noise floor. The SNR_{min} in turn is determined by the applied demodulation method to achieve a certain bit-error-rate (BER). Not knowing the required SNRmin a more straightforward way is to set the minimum tolerated input signal level based upon the 'F'. This defines the intermodulation-free dynamic range (IMFDR) parameter. When the maximum tolerated input signal level is based upon the amount of third-order intermodulation distortion (IMD_3) generated, the third-order IMFDR ($IMFDR_3$) parameter is defined. The $IMFDR_3$ equation given below is derived from [9].

$$IMFDR_3 = 2/3(IIP_3 - F_{IN}) \tag{1.2}$$

The IMD_3 products are close to the carriers when the carrier frequencies are chosen close together. Hence the IMD_3 products represents the dominant distortion contribution being located in-band. For being consistent with the linearity parameter the noisefloor should be referred to the input (F_{IN}). The concepts of linearity and noise are important during the research developments and discussed in {1.2.2} and {1.2.3}.

{Figure 3} is included to visualize the parameter relations previously discussed.

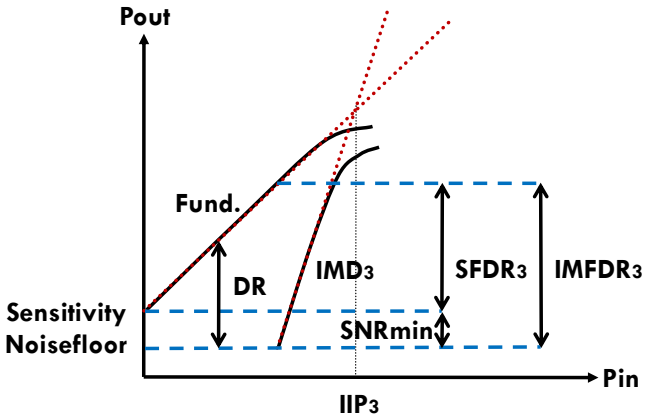

Figure 3: Parameter relations

1.2.2 Nonlinear distortion: The concept of (non-)linearity is introduced by the effect it causes namely signal distortion. Signal distortion, or shortly said distortion, actually refers to the distortion of a voltage- or current waveform as it is displayed versus time. In the frequency domain distortion is visible due to different spectral content in the input- and output signal. Both situations are illustrated in {Figure 4}.

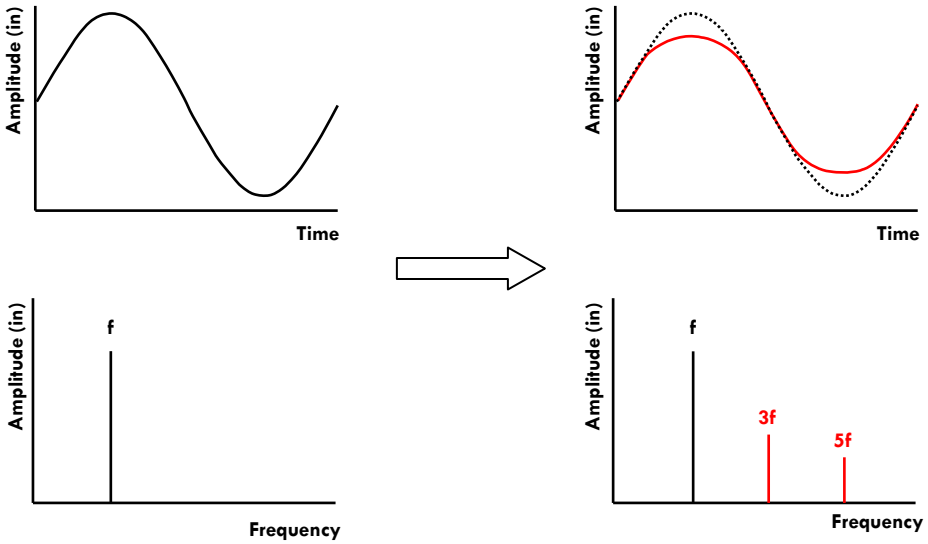

Figure 4: Distortion displayed in time- and frequency domain

Disperion is caused by signal filtering, resulting in subtraction of frequency contents from the original input signal. For instance when a square wave input signal is applied to a low pass filter (LPF). This type of distortion can be prevented for by keeping the signal bandwidth within the sytem bandwidth which is commonly considered.

Nonlinear distortion is caused by the application of an input signal upon a components nonlinear transfer characteristic resulting in the addition of frequency contents to the original input signal. This happens e.g. when a sinusoidal input signal is applied towards a metal-oxide-semiconductor transistor (MOST). This will result into a fundamental output tone and output frequency components at integer multiples of the fundamental input tone called harmonics. The nonlinear transfer characteristic causes variations in the small signal gain with the input signal strength, explaining the distortion origin in the time domain. This distortion type can be further subdivided into hard- and weak distortion. Hard distortion is created due to sharp edges in the nonlinear transfer characteristic. These sharp edges can be avoided with proper MOST biasing and reducing the input signal levels sufficiently. The gradual change in the MOST nonlinear transfer characteristic is intrinsic leaving weak nonlinear (WNL) distortion contributions as unavoidable, and the focus of further research.

The generation of frequency spurs due to a nonlinear transfer characteristic can be explained mathematically. The essential step is to translate the nonlinear transfer characteristic into a proper mathematical input-output relationship which is determined by the type of system. For a memoryless nonlinear system a polynomial function is a proper input-output representation. For a dynamic (memory) nonlinear system the impulse response (Volterra series) describes a proper input-output relationship. For the polynomial function a quick example is given on the next page.

$$y = a_0 + a_1 u + a_2 u^2 + a_3 u^3 \tag{1.3}$$

In the polynomial ‘y’ represents the output signal and ‘u’ the input signal. Coefficient ‘a_0’ represents the direct current component, ‘a_1’ the linear gain, ‘a_2’ the second-order distortion and ‘a_3’ the third-order distortion.

Higher order distortion components are neglected focussing upon WNL behavior and hence the polynomial is truncated. Assume we apply the following input signal and make use of two common trigonometric manipulations.

$$\begin{aligned} u &= U\cos(\omega t) \\ \cos^2 x &= 1/2(1+\cos 2x) \\ \cos^3 x &= 1/4(3\cos x + \cos 3x) \end{aligned} \tag{1.4}$$

Now the input-output relationship is transformed into the one given below. The last two terms clearly indicate harmonics generated.

$$y = \left(a_0 + \frac{a_2}{2}U^2\right) + \left(a_1 + \frac{3}{4}a_3 U^2\right)U\cos(\omega t) + \frac{a_2}{2}U^2\cos(2\omega t) + \frac{a_3}{4}U^3\cos(3\omega t) \tag{1.5}$$

Now the distortion can be quantified by watching the amount of harmonic content relative to the fundamental signal. The n-th order hardmonic distortion (HDn) is hence defined as the ratio of the component of frequency nω to the one at the fundamental frequency ω. Problem with the HDn parameter however is that for high fundamental frequencies the harmonics possibly are located outside of the system transfer characteristic. Due to the filtering action of the transfer characteristic the harmonics can be substantially attenuated representing the system more linear than it truly is. With a two-tone test in-band distortion is intentionally created to avoid the above issue. With similar mathematics it can be proofed to result in HD as well as IMD being all combinations of ω_1 and ω_2 and their multiples. The location of the IMD_3 products will be at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ which is very close to the fundamental tones when their frequencies are chosen close together. The IMD_3 however still requires specification of the input signal strength to be specific. A distortion parameter based upon the IMD_3 which doesn’t require specification of the input signal strength is the IIP_3. The IIP_3 specifies the input signal strength where the extrapolated curves of the fundamental- and IMD_3 component coincide {Figure 3}. The IIP_3 hence became the distortion parameter of choice.

Note that linearity is required for preventing distortion from in-band frequencies and filtering for out-band frequencies.

1.2.3 Noise: To be able to compare the noise performance of different circuits in a fair way the noise is generally referred to the input of the circuit [1]. This method to model the circuit noise generally requires a series voltages- and a parallel current source at the input of the circuit {Figure 5}. In case of a high circuit input impedance it is sufficient to use the series voltage source only, as in this particular case. The series voltage source is better known as the EIRNV and is the noise parameter used throughout this document. For convenience the EIRNV parameter represents a spotnoise value rather than a noise level value for which the spotnoise value should be integrated over the bandwidth of interest.

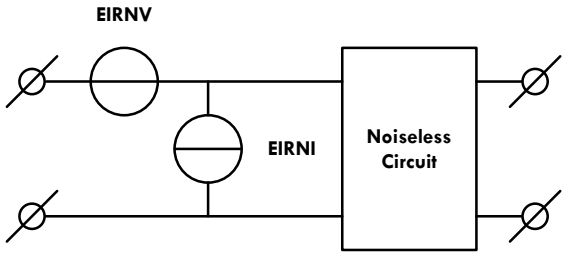

Figure 5: Circuit noise representation with ideal sources

Environmental noise stems e.g. from noisy supply lines and is not further addressed. This type of noise can be suppressed for by differential signalling which reduces the coupling effects.

Device noise stems from the active- and passive components within the circuit and can be further distinghuished into thermal- and flicker noise. Thermal noise is due to the random motion of electrons caused by temperature. The thermal noise is known for having a uniform noise spectral density which in amplitude is proportional to the temperature. MOSTs additionally generate flickernoise originating from the random trapping and detrapping of electrons at the oxide semiconductor interface due to the presence of dangling bonds. Flickernoise is frequency- rather than temperature dependent showing a noise spectral density inversely proportional to the frequency. Considering the design of an amplifier operating at intermediate frequencies the flickernoise contribution is neglected.

1.2.4 Feedback: In the specifications {1.1.2} it is only mentioned to design a fully differential amplifier with negative feedback and not the reason why. The reason is discussed here and starts from the Friis theory of cascaded circuits. This theory states that the gain of preceding stages downscales the noise and linearity of subsequent stages. Hence radio front-end blocks situated close to the antenna should primarily be designed for low noise and the ones at distant from the antenna primarly for high linearity. Since the amplifier is situated in the backend of the radio front-end high linearity prevails over low noise. The effect of feedback upon linearity and noise is discussed below to verify the choice made starting with the linearity.

Feedback can be subdivided into positive- and negative feedback [1]. Positive feedback is known for resulting into oscillatory behaviour which isn't desired when designing an amplifier. Hence feedback will refer to negative feedback in this document. Global negative feedback in particular since local negative feedback (e.g. emitter degeneration of a MOST) consumes large voltage headroom (low voltage technology) and decreases the already limited dynamic range even further. The feedback amplifier blockdiagram shown in {Figure 6} is an example of global negative feedback and used to explain the effect of feedback upon linearity.

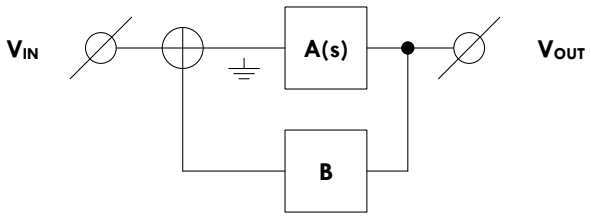

Figure 6: Feedback amplifier block diagram

When the feedback network ('B') doesn't load the gain stage (A(s)) the following well known equation is easily derived [1].

$$A_{CL}(s) = \frac{A(s)}{1 + A(s)B} = \frac{1}{B}\bigg|_{A(s)B=\infty} \tag{1.6}$$

In the above equation the closed-loop gain (A_{CL}) is determined by the feedback network when the loopgain (AB) is infinite. The feedback network is generally build from passive components which values can be controlled with high accuracy resulting in a constant gain with hence high linearity. The following observations are made;

- Use passive feedback components since nonlinearities aren't suppressed here
  - Use an Op Amp gain stage (large A) with large feedback factor (B)
- Linearize the Op Amp gain stage for less dependence upon the loopgain.

The effect of feedback upon the noise performance is determined with the block diagram depicted in {Figure 7}. Here the Op Amp noise is represented by the input referred noise voltage source 'V_N' and the feedback network itself is assumed noiseless.

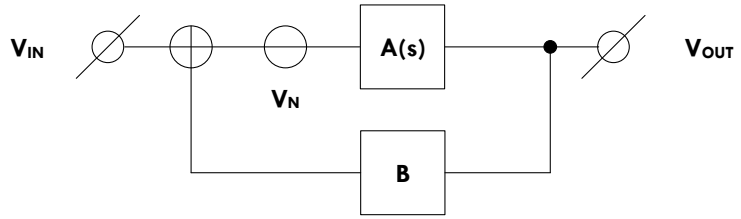

Figure 7: Feedback amplifier block diagram with Op Amp noise represented by 'V_N'

For this circuit the following equation can be derived [1]

$$\frac{V_{OUT}}{(V_{IN}+V_N)} = \frac{A(s)}{1+A(s)B} = \frac{1}{B}\bigg|_{A(s)B=\infty} \tag{1.7}$$

Clearly the Op Amp input-referred noise becomes the amplifier input-referred noise and no effect upon the noise performance is seen. In reality the feedback network will degrade the overall noise performance due to the addition of noise from the feedback network components themselves which should therefore be kept small.

Expecting strong effect upon the linearity performance with negligible effect upon the noise performance application of feedback seems appropriate for high $IMFDR_3$ design. Additional appealing aspects of feedback like terminal impedance- and bandwidth modification further strengthened this choice.

1.3 Thesis outline:

Chapter {1}: “Introduction”. This chapter entails a project description, literature review and thesis outline to familiarize the reader with the main topics.

Chapter {2}: “Basic amplifier topology for high $IMFDR_3$”. Here the goal is to present an amplifier circuit with a high $IMFDR_3$ potential. As such this chapter will explain the choices made before ending up with the final topology used. Having determined the final topology, a quick biasing and dimensioning procedure will follow to perform functionality- and performance checks.

Chapter {3}: “SC-FDA *analysis* for high $IMFDR_3$”. Here research is conducted to determine the bias and dimension for the topology for high $IMFDR_3$. For this the major distortion- and noise locations will be determined and methods proposed for optimization.

Chapter {4}: “SC-FDA *design* for high $IMFDR_3$”. Here the research results from chapter 3 are applied on the topology from chapter 2, for high $IMFDR_3$ design. The applied design procedure is discussed, after which the circuit will be simulated to determine the final specifications. The final specifications will then be compared with the initial specifications to reflect upon the efforts made.

Chapter {5}: “Conclusions and Recommendations” will give the most important conclusions and recommendations for future work and is the final chapter of this report.

2 Basic amplifier *topology* for high $IMFDR_3$:

The aim of this project is the design of a high $IMFDR_3$ amplifier with proper mixer interfacing. Hence a topology should be proposed first which is done in this chapter. Since parts of the circuit are still ideal the amplifier topology is referred to as being a basic amplifier topology for high $IMFDR_3$, explaining the chapter title.

2.1 Introduction:

In this chapter the basic amplifier topology is determined. Starting from a reference circuit {2.2.1} the structure is modified for proper mixer interfacing {2.2.2} and added with common-mode circuitry {2.2.3} before ending up with the final topology used. The final topology is then subjected to a quick biasing and dimensioning procedure {2.3} to be able to conduct functional- and performance testing {2.4}. The functional- and performance testing is needed to verify if the circuit operates properly and has indeed a high $IMFDR_3$ potential. At the end of this chapter a brief summary {2.5} is given before proceeding with the actual research in chapter {3}.

2.2 Topology:

2.2.1 Reference circuit: In {1.2.4} the attention is directed towards a low distortion feedback Op Amp design as proposed in [5] and [10]. The design of the amplifier is discussed here starting with the feedback network and followed by the Op Amp.

Although having better IMD_3 performance the differential amplifier proposed is implemented fully differential as required from specification {1.1.2} considering the following additional aspects [1].

- Suppressing even-order distortion
- Increase of the DR due to larger allowed signal swings
- Reduction of signal corruption due to coupling

The amplifier will be connected in inverting configuration because fully differential non-inverting amplifiers simply do not exist [12]. This is also proposed [5] for higher linearity regarding single-ended amplifiers. Knowing that nonlinearities in the feedback network aren't suppressed [4] the feedback network components should be linear and hence be implemented with passive components. The feedback network was initially implemented with resistors as depicted in {Figure 8}.

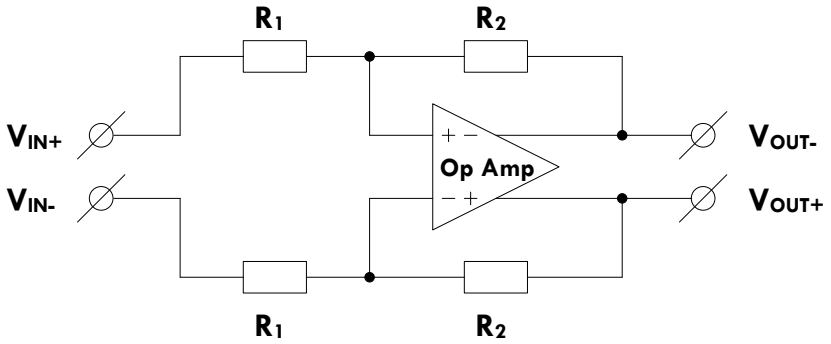

Figure 8: Fully differential amplifier with resistive feedback

The closed-loop gain is determined by the feedback resistor ratio indicated below.

$$A_{CL} \approx -\frac{R_2}{R_1} \tag{2.1}$$

The proposed Op Amp is the folded cascode Miller Op Amp with common source output stage displayed in {Figure 9}. Two-stage designs have isolated gain and swing not provided for by single-stage designs. Designs with more than two stages have increased stability problems complicating design. Since each stage introduces at least one pole and each pole ultimately a phase shift of 90 degrees the problem of instability arises [1]. For stability the amplifier is forced to act like a one-pole system up to its unity gain frequency (UGF) with Miller frequency compensation capacitors (C_C).

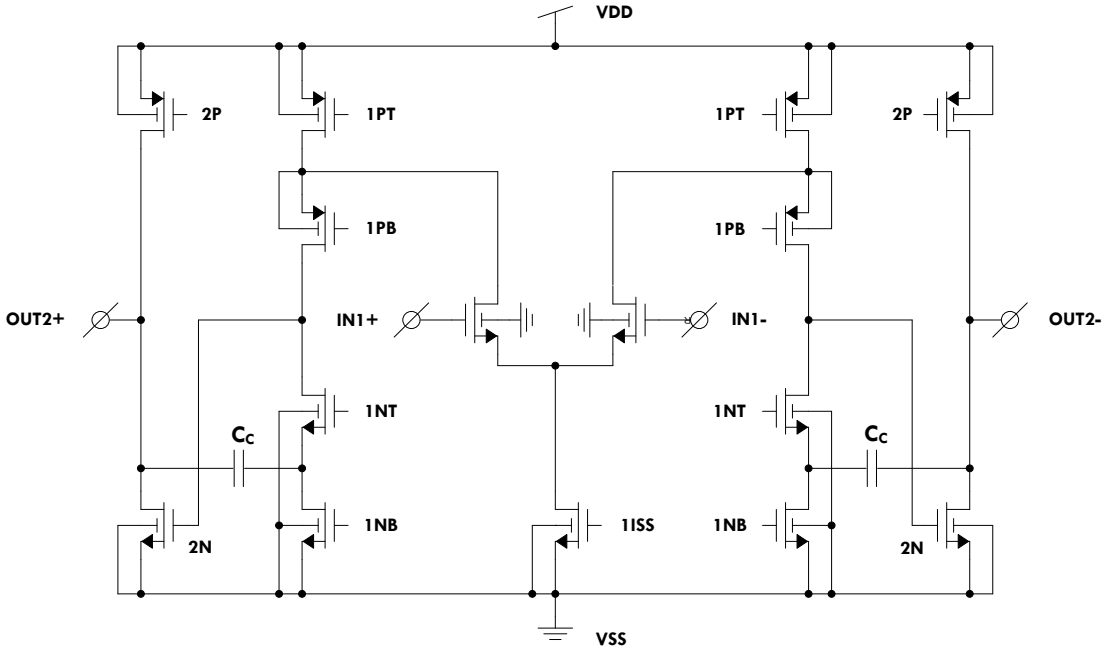

Figure 9: Folded cascode Miller Op Amp with common source output stage

The folded cascode input stage is very popular in low voltage technologies like CMOS 65nm. The folding creates additional voltage headroom which translates into less MOST distortion [5]. The input stage gain is given below [1].

$$\begin{aligned} A_1 &= -gm_{1IN} R_{OUT1} \\ R_{OUT1} &= R_{PMOS} \,||\, R_{NMOS} \\ R_{PMOS} &= gm_{1PB} ro_{1PB} (ro_{1PT} \,||\, ro_{1IN}) \\ R_{NMOS} &= (gm_{1NT} + gmb_{1NT}) ro_{1NT} ro_{1NB} \end{aligned} \tag{2.2}$$

The common source output stage is a common driver stage allowing rail-to-rail operation and hence high dynamic range. The output stage gain is given now [1].

$$\begin{aligned} A_2 &= -gm_{2N} R_{OUT2} \\ R_{OUT2} &= ro_{2N} \,||\, ro_{2P} \end{aligned} \tag{2.3}$$

The Miller frequency compensation choice should yield better linearity performancethan other frequency compensation methods due to the negative feedback involved [13]. Additionally the Miller capacitance is multiplied by the gain of the shunted stage resulting into practical on-chip capacitor values. Neglecting parasitic capacitances the following pole locations can be determined [1].

$$\begin{aligned} \omega_1 &\approx \frac{1}{gm_{2N} R_{OUT2} C_C R_{OUT1}} \\ \omega_2 &\approx \frac{gm_{1NT} gm_{2N} R_{OUT1}}{C_L} \\ \omega_z &\approx \frac{gm_{1NT} gm_{2N} R_{OUT1}}{C_C} \end{aligned} \tag{2.4}$$

For a one-pole system the transfer function shows a 20dB/dec or 6dB/oct slope decent starting from the dominant pole- upto the UGF location. Therefore the UGF can be determined from the dominant pole location after multiplication with the Op Amp gain.

$$UGF \approx \frac{gm_{1IN}}{C_C} \tag{2.5}$$

Desiring ≥ 12dB gain and ≥ 25MHz bandwidth {1.1.2} forces UGF ≥ 100MHz.

2.2.2 Interfacing: This section is about realizing proper interfacing with the preceding mixer stage which has a differential S&H output {Figure 10}. The mixer output capacitors should be maintained at steady voltages for proper circuit operation. Hence the amplifier should have a high input impedance for preventing mixer loading.

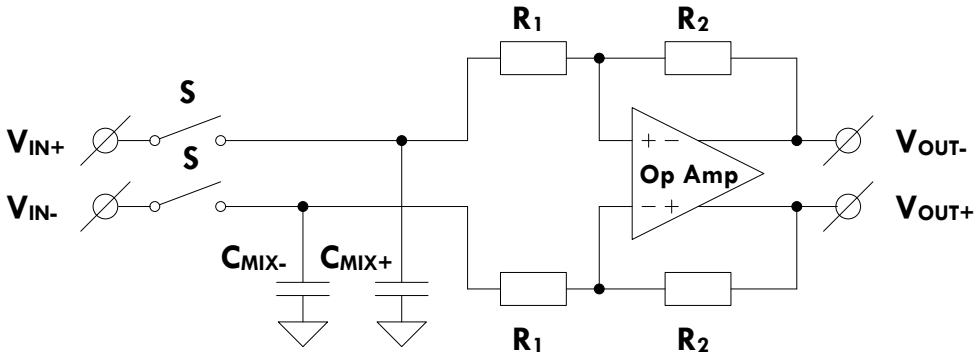

Figure 10: Mixer-Amplifier interfacing with resistive feedback

Recognizing the Op Amp inputs as virtual ground nodes the amplifier input impedance equals R_1 single-ended and $2\times R_1$ differential. Addionally R_2 must scale with R_1 regarding the desired A_{CL}. Now the problem with using large feedback network resistors is the noise generated. The noise of R_1 is already referred to the input- and of R_2 to the output of the amplifier. The noise of R_2 can be referred to the input of the amplifier after division with the A_{CL}^2. Assuming a noiseless Op Amp itself the following equation can be derived based upon the fact that the noise sources are uncorrelated and stochastic and hence their individual powers add.

$$\overline{V_N^{\,2}} = \overline{V_N^{\,2}, R_1} + \frac{\overline{V_N^{\,2}, R_2}}{A_{CL}^{\,2}} = 5kTR_1$$
$$P_{AV}, balanced = 2P_{AV}, unbalanced \quad [1]$$
$$\overline{V_N^{\,2}, balanced} = 10kTR_1 \tag{2.6}$$

From the specifications {1.1.2} the EIRNV should be ≤ 3nV/√Hz.

$$P_{AV} = P_{RMS}^{\,2} \quad [1]$$
$$\overline{V_N^{\,2}, balanced} \le (3\times10^{-9})^2 \le 9\times10^{-18} V^2/Hz$$
$$10kTR_1 \le 9\times10^{-18} \tag{2.7}$$
$$R_1 \le 217\Omega \rightarrow R_2 \le 868\Omega$$

This are the maximum feedback network resistor values usable based upon the noise specification using a noiseless Op Amp. In reality the input-referred Op Amp noise still adds directly to this noise {1.2.4} requiring even smaller feedback network resistor values. Clearly the amplifier will start loading the preceding mixer circuit and the feedback network the Op Amp, both being undesired. Based upon these considerations capacitive feedback is proposed as shown in {Figure 11}.

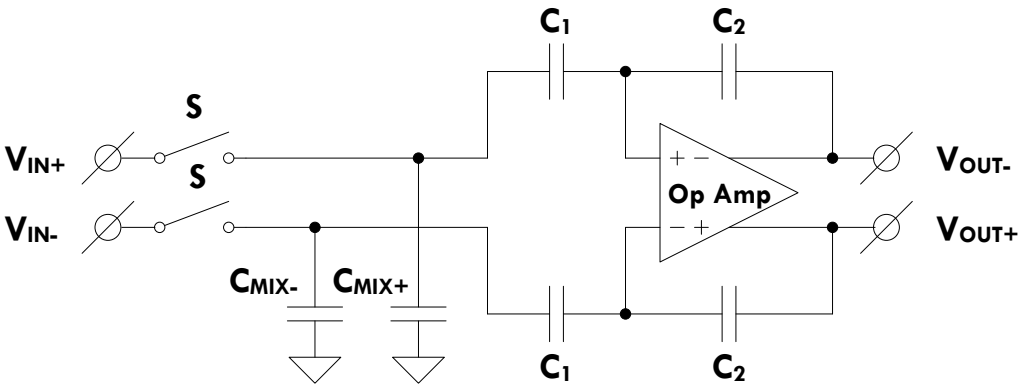

Figure 11: Mixer-Amplifier interfacing with capacitive feedback

Now capacitors are generally known for having high quality factors (Q_C) and hence small equivalent series resistance (ESR) resulting into negligible noise contribution from the feedback network. Additionally for intermediate frequencies and small on-chip capacitor values realizing a high amplifier input impedance seems possible. The input impedance versus noise trade-off, so prevalent regarding resistive feedback, doesn't exist anymore being the great advantage. The closed-loop gain is still determined by the ratio of the feedback network components and hence frequency independent. The ratio is opposite compared to the resistive feedback case as indicated in the equation below.

$$A_{CL} \approx -\frac{C_1}{C_2} \tag{2.8}$$

2.2.3 Common-mode circuitry: For the capacitive feedback network displayed in {Figure 11} the Op Amp input common-mode voltages are poorly defined. The feedbacknetwork capacitors create a high impedance node explaining the situation. Recognizing discrete-time operation for the preceding mixer circuit, switched biasing is considered as shown in {Figure 12} resulting into a discrete-time operated amplifier as well. The switched biasing proposed differs from suggested [1], allowing different Op Amp input- and output common-mode voltages as generally desired.

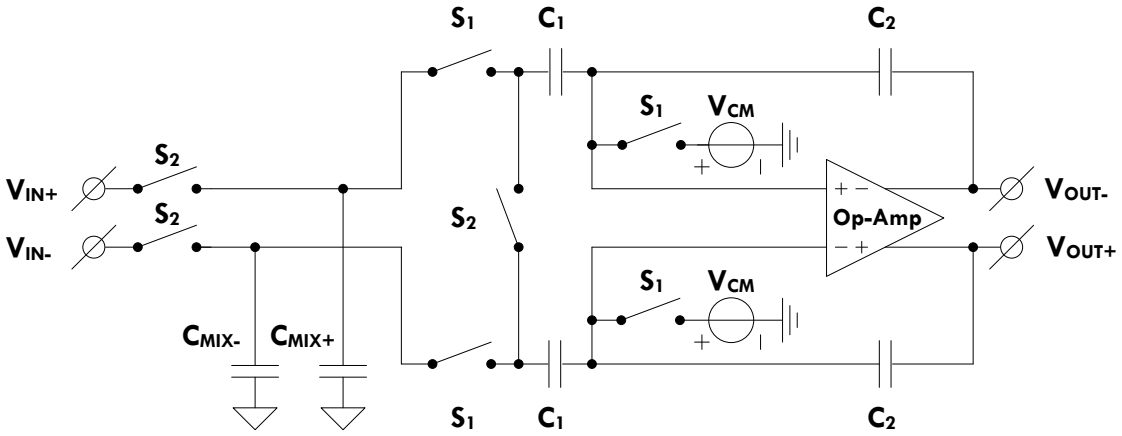

Figure 12: Switched-capacitor amplifier concept

The design of a discrete- rather than continuous-time operated amplifier offers significant advantage knowing that switched-capacitor (SC) circuits are generally based upon voltage settling. This means that there is no current flowing through the feedback network capacitors anymore (at the end of the amplification phase) and hence no loading from the feedback network upon the Op Amp exists. This results into higher loopgain, creating larger distortion suppression and hence higher circuit linearity. {Figure 13} is a slightly more detailed version of {Figure 12}. The additional switches at the stages ouputs prevent systematic offsets.

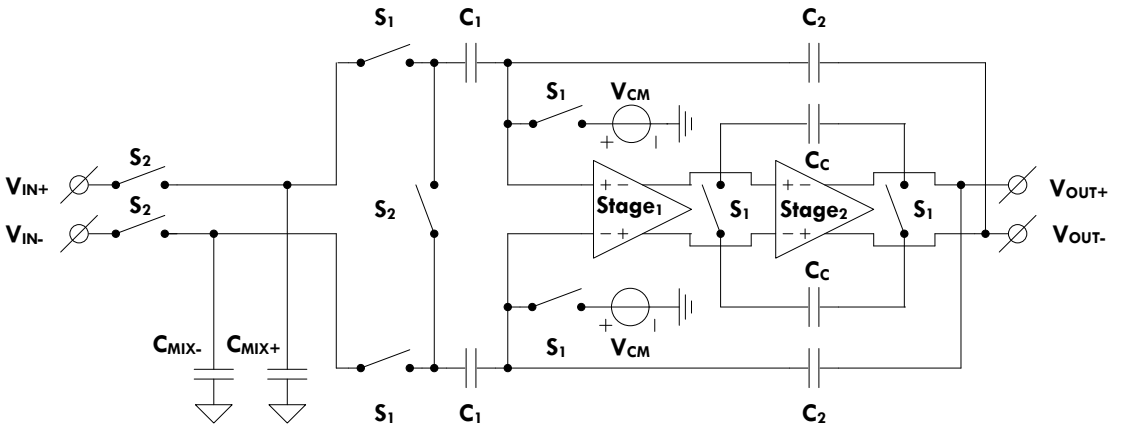

Figure 13: Switched-capacitor amplifier implementation

A general explanation for SC circuits operation is based upon the charge conservation law arising from fundamental physics [1]. Essential is realizing that the circuit configuration is fundamentally different in both clock phases. Starting at clock phase 'S_1' all S_1 switches are closed and 'S_2' switches are opened. Now the switched biasing

is connected realizing a differential-mode ground and a common-mode bias at the Op Amp inputs. This results into the sampling of the mixer signal upon the amplifier input capacitors and the unloading of the amplifier output capacitors. The mixer signal sampled and the amplifier output capacitors unloaded where already established during the previous (and also subsequent) clock phase 'S_2'. Hence revealing a cyclic circuit operation consisting of two clock phases. Effectively the mixer output capacitors and the amplifier input capacitors are placed in parallel during the sampling operation. This resuls into a certain charge withdraw from the mixer capacitors being placed upon the amplifier input capacitors.

During the next clock phase 'S_2' all S_2 switches are closed and 'S_1' switches are opened. Now the switched biasing is disconnected, creating a floating node for common-mode signals, keeping the potential relatively constant. The switched biasing periodically refreshes the potential upon this node to compensate for small leakage currents. More remarkable is the influence upon the differential-mode signals. The differential-mode voltage previously present on the left most feedback network input capacitors plates is initially redirected towards the inner feedback network capacitors plates. The feedback through the amplifier output capacitors is known to suppress the differential-mode voltage upon this node. So the Op Amp output is driven by the initial Op Amp input differential-mode voltage to effectively remove the charge from the inner plates. This charge is now redirected towards the right most feedback network output capacitors plates, while still obeying the charge conservation law. From the previous equation it is obvious that placing the same amount of charge on a two times smaller capacitor yields a two times higher voltage. Clearly the amplification of the circuit is still determined by the ratio of the feedback network components as was previously the case. Each clock period one signal is processed over and over again while amplified with the gain set by the feedback network capacitors ratio indicated below.

$$V_{OUT}(s_2) = -V_{IN} \quad s_1 \quad \frac{C_1}{C_2} \tag{2.9}$$

Comparable problems reside inside both Op Amp stages again requiring additional circuitry. Both Op Amp stages have a high output impedance for realizing gain again resulting in poorly defined output common-mode voltages. Generally these high impedance nodes can be spotted where MOSTs are connected drain to drain. The problem is discussed with the help of {Figure 9} being the schematic of the Op Amp used. Here at the output nodes of the output stage the current sourced by the top PMOST (2P) device is never exactly balanced by the current drained by the bottom NMOST (2N) device. The resulting mismatch current will flow into the output nodes having high impedance. Hence the common-mode voltage at these nodes will be increased/decreased depending upon which current is larger 2P/2N resulting into a poorly defined output common-mode voltage. To define proper common-mode voltages upon these nodes common-mode feedback (CMFB) is needed. For fully differential circuits this function is performed with common-mode feedback networks. Two CMFB implementations will be discussed, one for each stage, starting with the input stage. The input stage is designed for high gain and hence capacitive common-mode sensing is preferred for not reducing the output impedance. Based upon the discrete- time operation of the amplifier and the desire for accurate output common-mode levels SC-CMFB is proposed [1] as shown in {Figure 14}.

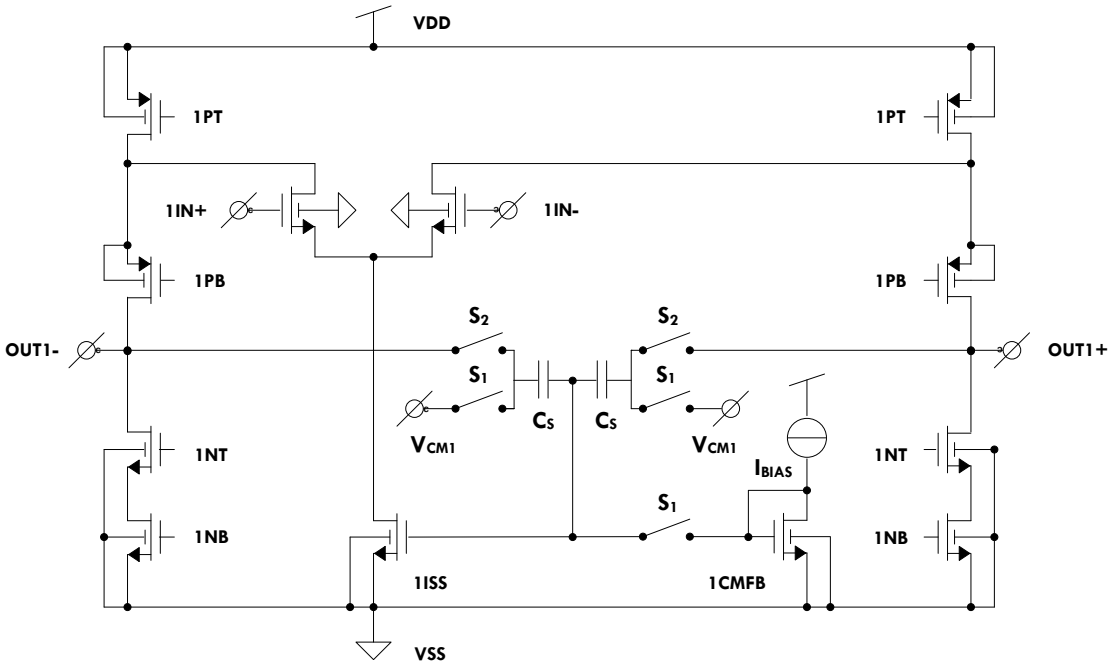

Figure 14: Input stage with SC-CMFB

In clock phase 'S_1' only the sensing capacitors (C_S) are periodically refreshed and the SC-CMFB network has no effect. The voltage placed upon the sensing capacitors acts as a dc-shift in clock phase 'S_2'. During clock phase 'S_2' the SC-CMFB network is connected with the output nodes and the tail current source. Now acting as a self-stabilizing system, known for negative feedback operation, upon the common-mode output voltages. When the output common-mode voltage is higher/lower than 'V_{CM1}' the gate voltage of the tail current source will be increased/decreased regarding the situation at 'S_1'. This results into less/more current sourced into the output nodes considering '1PT' as a constant current source. With the current drained by the '1NB' MOSTs constant the output common-mode voltages will hence be lowered/raised. Equilibrium is reached when the output common-mode voltages approach 'V_{CM1}'. The SC-CMFB operation is simplified in {Figure 15} where the comparator block replaces the charged sensing capacitors [14].

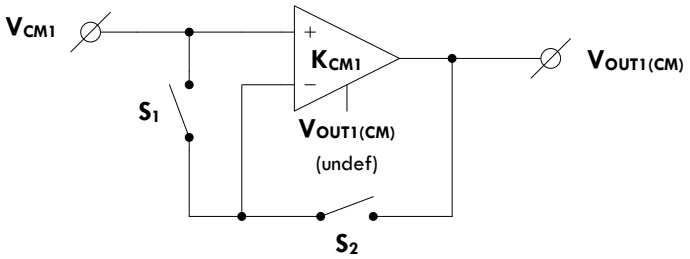

Figure 15: SC-CMFB

During clock phase 'S_1' there is no negative feedback and '1OUT_CM (def)' equals '1OUT_CM (undef)'. For clock phase 'S_2' the following derivation can be made.

$$V_{OUT1(CM)} = V_{OUT1(CM)(undef)} + K_{CM1}(V_{CM1} - V_{OUT1\_CM})$$
$$V_{OUT1(CM)} = V_{CM1}\big|_{K_{CM1}=\infty} \qquad (2.10)$$
$$K_{CM1} = -gm_{1ISS}R_{OUT1}$$

The output stage is designed for high signal swings c.q. low gain considering the lack of stacked MOST devices. Hence resistive common-mode sensing is appropriate and applied as suggested in [1] and shown in {Figure 16} below.

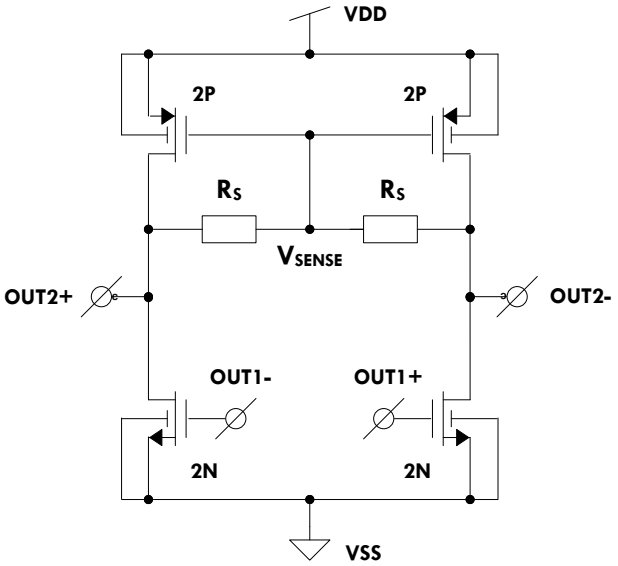

Figure 16: Output stage with R-CMFB

Essential is to recognize the PMOST as a diode connected device for common-mode signals resulting into bias voltage generation. The bias voltage generated will be compared with the common-mode voltage being sensed with the sensing resistors (RS). Ideally differential-mode signals have no effect upon the common-mode voltage regulation. The R-CMFB operation is simplified in {Figure 16} below.

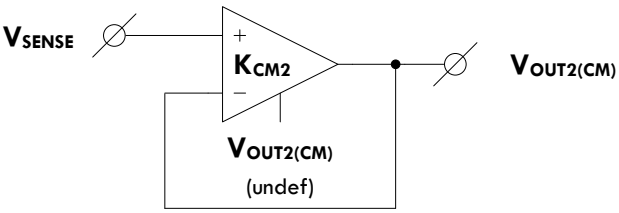

Figure 17: R-CMFB

$$V_{OUT2(CM)} = V_{OUT2(CM)(undef)} + K_{CM2}(V_{SENSE} - V_{OUT2(CM)})$$
$$V_{OUT2(CM)} = V_{SENSE}\big|_{K_{CM2}=\infty} \qquad (2.11)$$
$$K_{CM2} = -gm_{2P}(ro_{2P} \,||\, ro_{2N}) \approx -1 \rightarrow V_{SENSE} = V_{BIAS}$$

The sensing node (V_{SENSE}) is a virtual ground node for differential-mode signals and hence R-CMFB is effecting the differential-mode gain of the output stage as expected and indicated in the equation below. This isn't the case for SC-CMFB networks due to the high reactance of the used sensing capacitors.

$$A_2 = -gm_{2N}R_{OUT2}$$
$$R_{OUT2} = ro_{2N} \,||\, ro_{2P} \,||\, R_S \qquad (2.12)$$

2.2.4 Testbench: For simulating fully differential circuits the testbench displayed in {Figure 18} is proposed [15]. Essential is to make use of baluns to transform unbalanced- into balanced signals and visa versa. The left block represents the amplifier of {Figure 13} and the right rectangle the ideal sample-and-hold (S&H) circuit displayed in {Figure 19}.

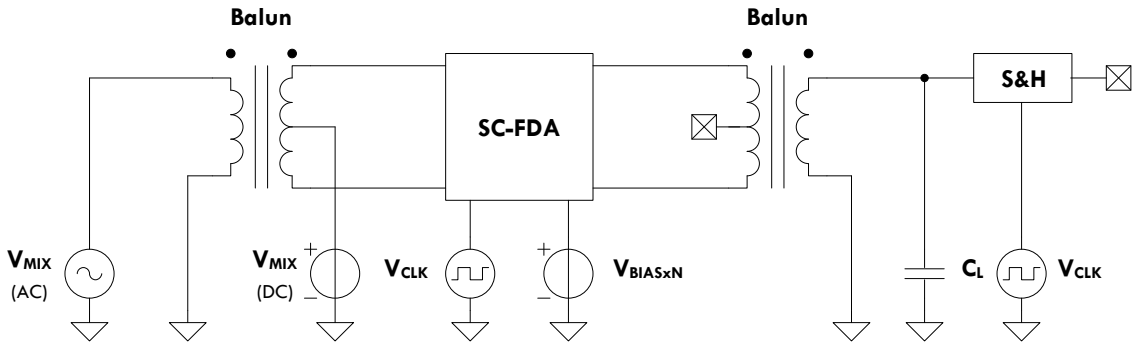

Figure 18: Testbench for fully differential circuits

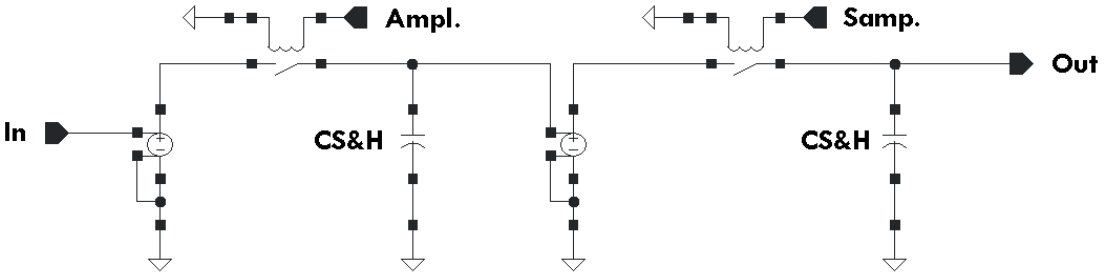

Figure 19: Ideal S&H circuit

The amplifier output signals are directed through the ideal sample-and-hold circuit to separate the desired signal from the settling behaviour. By doing so the discrete-time signal is transformed into continuous-time again as can be seen in {Figure 23}. The capacitor in front of the sample-and-hold circuit represents the capacitive load (C_L) which is typically chosen 1pF. Further the supply voltage is implemented unipolar since bipolar supplies require two batteries increasing the formfactor. Finally the clock frequency is set at 200MHz which is the minimum clock frequency allowed for direct connection with the preceding mixer stage [7]. Minimum clock frequency translates into maximum clock periods c.q. -phases giving voltage settling more time to be accomplished. Clearly this allows larger amplifier gains for increased $IMFDR_3$ performance considering the gain versus bandwidth tradeoff.

2.3 Biasing and Dimensioning:

2.3.1 Biasing: With the topology determined the biasing should be considered to allow intial- functionality- and performance testing. Regarding the biasing the initial-voltages and currents will be assigned to operate all MOSTs in saturation region. In linear region the gain is reduced and in weak inversion the dynamic range and bandwidth (due to limited biasing currents) explaining the choice made.

Voltages: The supply voltage is determined by the integrated circuit technology used at 1.2V and implemented unipolar. All NMOST bulk contacts are at ground pontential considering standard integrated circuit processing {1.1.2}. The PMOST bulk contacts are shorted with the corresponding source contacts to keep the threshold voltage low being a practical consideration for low voltage design. All remaining MOST contacts are biased for operating the MOSTs in saturation region as already said. For a NMOST this means that the minimum gate voltage is a threshold voltage above the source voltage and the maximum gate voltage is a threshold voltage above the drain voltage. This way the on average needed gate voltage is determined and applied for safe operation [For a PMOST the maximum gate voltage is a threshold voltage below the source voltage and the minimum gate voltage is a threshold voltage below the drain voltage]. The determination of the threshold voltage in turn is done with ProMOST specifying CLN65SVTa13 NXP 2008 as the used MOST type. The dominant parameters in the determination of the threshold voltage were found to be the MOST type and the applied bulk-source voltage, luckily being both already assigned. The drain-source voltages are futher evenly distributed within the circuit by equal division with the number of stacked devices. The remaining mixer-amplifier interface voltage was set at 750mV for expected linearity considerations.

Currents: The circuit power dissipation is determined by the product of the supply-voltage and current. With the supply voltage fixed at 1.2V the power dissipation becomes completely determined by the supply current drawn. Higher branch currents will result into higher linearity performance considering lower relative current swings. Addtionally higher branch currents will result into lower noise as well based upon admittance level scaling. Hence it is determined to use the maximum power budget of 10mW {1.1.2}, for designing a high $IMFDR_3$ amplifier, being translated into a maximum supply current drawn of 9mA for a 1.2V supply voltage. In the Op Amp six effective current branches can be distinguished. Neglecting the current mirror voltage biasing branch in the input stage being possible to be realized for very low power consumption. With six current branches and 9mA supply current present it is decided to set each branch current equal to 1.5mA in advance. This automatically resulted into a 3mA branch current for the tail current source and both PMOST current source branches/devices in the input stage. Negligible power is dissipated in the feedback network being blocked by the feedback network capacitors and hence not futher considered.

The initial voltage- and current biasing for the amplifier Op Amp stages is displayed in appendix {B} for which the upper values should be considered. The lower values are regarding the final design discussed in chapter {4}.

2.3.2 Dimensioning: With the topology determined the dimensioning should be considered to allow initial- functional and performance testing. Regarding the dimensioning the initial- active and passive component values will be assigned. Starting with small dimensioning voltage settling is reasonably assured as desired.

Actives: The dimensioning of the active components starts by specifying the MOST length. The MOST width then automatically results due to the previously assigned biasing conditions. Further the MOST length is limited to integer scaled values of the minimum MOST length regarding layout considerations [1]. The minimum MOST length equals 60nm for 65nm technology as verified with ProMOST. The actives dimensioning is started at the Op Amp output stage, for convenience at device 2N. Since assignment of 60nm MOST length resulted into insufficient gain for the output stage this value is doubled towards 120nm. This determined the 2P MOST length to be chosen equal to 180nm for having comparable output impedance. The NMOSTs- and PMOSTs lengths in the input stage where chosen equal to the output stage lengths considering the upcoming linearity research. Different MOST lengths are expected to render different distortion results as later verified.

Comp.	W (um)	L (um)	gm (mS)	gmb (mS)	rds (Ω)	Vth (mV)	Vdsat (mV)
2P	*224.3*	*0.18*	*16.1*	*-x-*	*1573*	*455*	*180*
2N	*81.27*	*0.12*	*16.9*	*-x-*	*1363*	*420*	*180*
1PT	*525.0*	*0.18*	*32.7*	*-x-*	*450*	*455*	*175*
1PB	*262.5*	*0.18*	*16.3*	*-x-*	*899*	*455*	*175*
1NT	*128.9*	*0.12*	*19.1*	*2.6*	*768*	*465*	*167*
1NB	*98.67*	*0.12*	*17.5*	*-x-*	*821*	*425*	*175*
1IN	*90.92*	*0.12*	*17.1*	*2.2*	*1056*	*480*	*180*
1ISS	*177.2*	*0.12*	*34.4*	*-x-*	*554*	*420*	*180*
1BIAS	*165.0*	*0.12*	*33.9*	*-x-*	*660*	*420*	*180*

Table 1: Initial active component values

Passives:

Comp.	Value	Determined
C_L	*1pF*	*Typical*
Ropen_switch	*1TΩ*	*Ideal*
Rclosed_switch	*1Ω*	*Ideal*
C_1	*1pF*	*Maximum mixer loading*
C_2	*250fF*	*Maximum loopgain*
C_C	*1pF*	*(2.4.1)*
C_S	*500fF*	*(2.4.1)*
R_S	*1600Ω*	*(2.4.1)*
$C_{S\&H}$	*250fF*	*(2.4.1)*

Table 2: Initial passive component values

The initial actives- and passives dimensioning for the amplifier Op Amp stages is displayed in appendix {C} for which the upper values should be considered. The lower values are for the final design discussed in chapter {4}. Additional device information is given in {Table 1} and {Table 2} with for some passives the way they are determined.

2.4 Testing:

2.4.1 Functionality: The functionality testing initially focusses upon the determination of the remaining passive component values listed in {Table 2}. Then with all active- and passive component values known proper biasing conditions should be verified first. Being trivial, except for the switched biasing maybe, these results aren't reproduced to prevent document overhead. Instead the SpectreRF biasing conditions are assumed in close agreement with ProMOST when the simulated- match the calculated gains as verified in {Table 3}.

Miller capacitors: The Miller capacitors are applied to perform frequency compensation within the differential-mode feedback network and hence should be determined by stability considerations. Direct stability simulations inside SpectreRF aren't applicable due to the existence of multiple non-touching loops [17]. Luckily for large signal applications time domain simulations proof more relevant [1] demanding step response analysis. First the remaining passive components are assigned an average on-chip value to be able to run a simulation anyway. For the capacitors 0.5pF and for the resistors 1.6kΩ values were chosen. Later values are expected, if necessary forced, to have comparable values. The stepresponse simulation result is displayed in {Figure 20} for a 150mV input signal. Clearly the Miller capacitors should be chosen 1pF for quick voltage settling while realizing a stable first-order response.

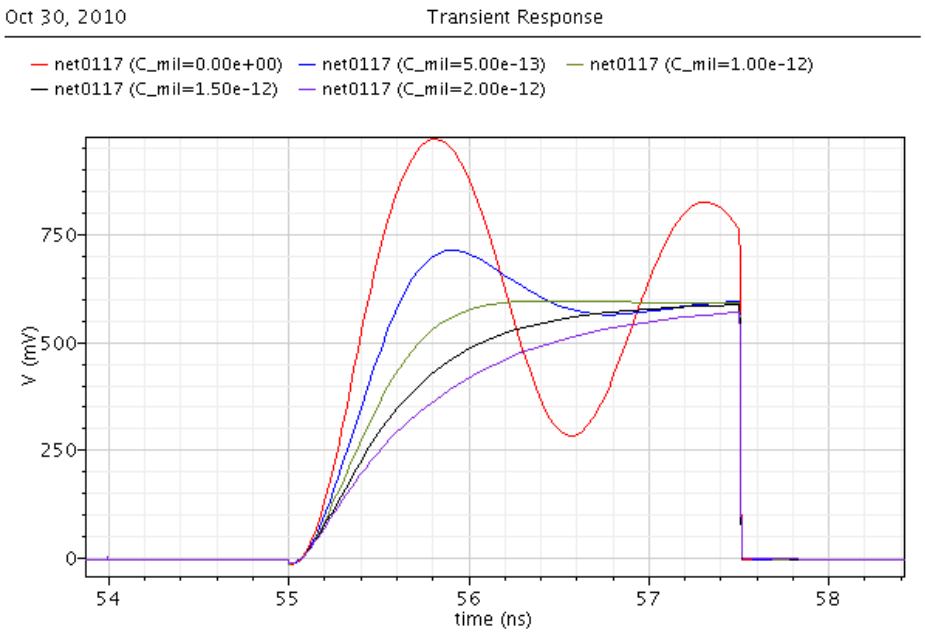

Figure 20: Step signal response

SC-CMFB sensing capacitors: The SC-CMFB loop in the input stage lacks frequency compensation and therefore stability is simply assumed. The sensing capacitors are now chosen based upon realizing common-mode voltage settling with practical on-chip component values. In {Figure 21} common-mode voltage settling is viewed for 'C_S' values above 500fF. The 'C_S' value is therefore chosen equal to 500fF.

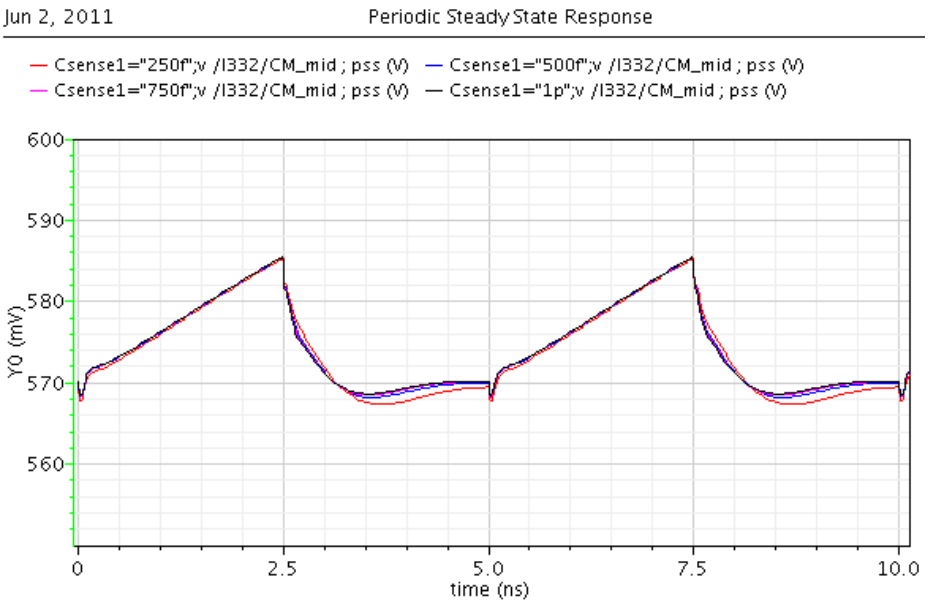

Figure 21: Common-mode voltage settling by SC-CMFB network

R-CMFB sensing resistors: Similar reasoning for the SC-CMFB loop applies for the R-CMFB loop. However here the sensing resistors aren't only based upon realizing common-mode voltage settling with practical on-chip component values but also on realizing an average output stage gain. In {Figure 22} common-mode voltage settling is viewed for 'R_S' values below 2kΩ. The 'R_S' value is chosen 1k6Ω for realizing an average output stage gain of 8.5 times.

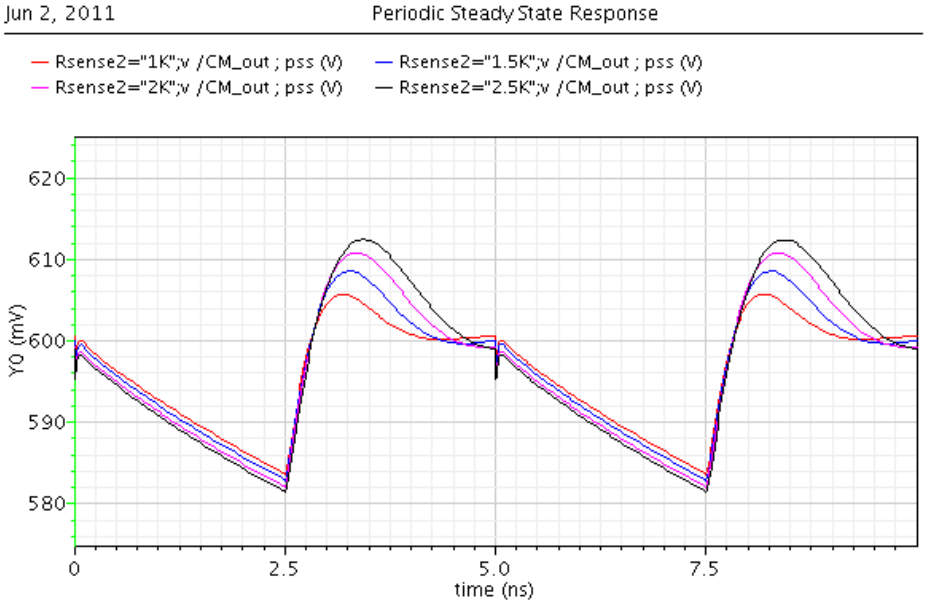

Figure 22: Common-mode voltage settling by R-CMFB network

S&H capacitors: The S&H operation displayed in {Figure 23} is based upon using 250fF S&H capacitors. Due to the ideal voltage controlled voltage sources (VCVS's) used in {Figure 19} the exact capacitor values can be chosen rather arbitrarily.

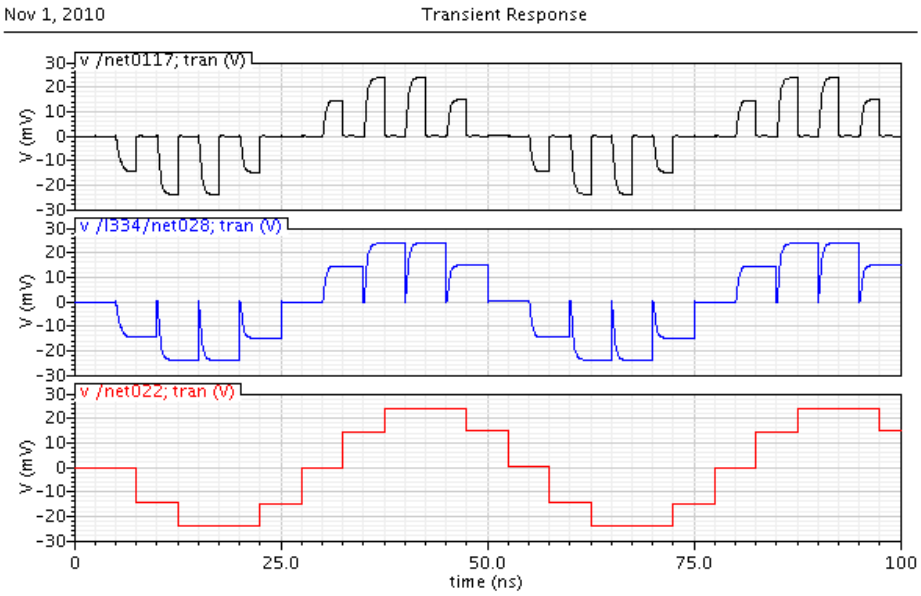

Figure 23: S&H operation

A_{CL}, A_1 and A_2: In {Figure 24} the amplifier input- and output signals are displayed together with the stages input- and output signals (obtained with the S&H circuit displayed in {Figure 19}). From the simulation results displayed the simulated gains are determined. The calculated gains are determined with equations {2.2}, {2.3} and {2.10} using the component parameters in {Table 1} and {Table 2}. {Table 3} summarizes the results for a quick comparison.

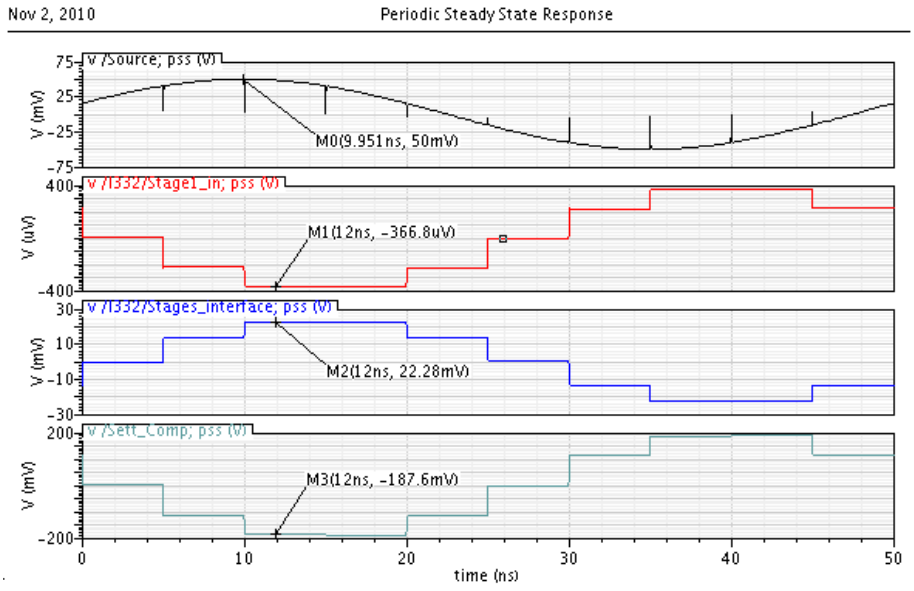

Figure 24: Amplifier voltage waveforms

	Sim.	Cal.
A_1	*-60.7*	*-66.6*
A_2	*-8.4*	*-8.5*
A_{CL}	*-3.95*	*-4.00*

Table 3: Simulated- and calculated gains

Due to the fact that MOST '1PT' has a 10 times higher output impedance than MOST '1PB' the signal current flowing towards the input stage output node is reduced by 10% giving 10% gain reduction. This factor wasn't anticipated for in the input stage gain equation explaining the difference. Due to the fact of 100 times loopgain the closed-loop gain shows a relative gain error of 1%. Based upon {Table 3} and the previous explanations proper circuit biasing and functionality is assumed.

2.4.2 Performance: The performance testing focusses upon the determination of the initial specifications. Before proceeding with the topology chosen the actual specifications are compared with the listed specifications {Table 4} to determine if the circuit has serious- potential or shortcommings. Not only the actual performance results but also the manner they were obtained is discussed.

IIP_3: For linearity determination the two-tone test is performed to derive the IIP_3 value. Key is to apply the right test-tone frequencies while the amplitude is being swept. The test-tone frequencies chosen are 20MHz and 25MHz. Due to the ideal feedback network the applied test-tones will be within the system bandwidth as desired. Additionally the test-tone frequencies are low enough for providing sufficient oversampling ratio (OSR) resulting into representive amplifier output signals. With these particular frequencies HD and IMD will not coincide giving proper results as displayed in {Figure 25}. Quasi-periodic steady-state (QPSS) analysis is performed rather than periodic steady-state (PSS) analysis for better simulation convergence and reduced simulation time. The derived IIP_3 value of 20.7dBm proofs adequate {1.1.2}.

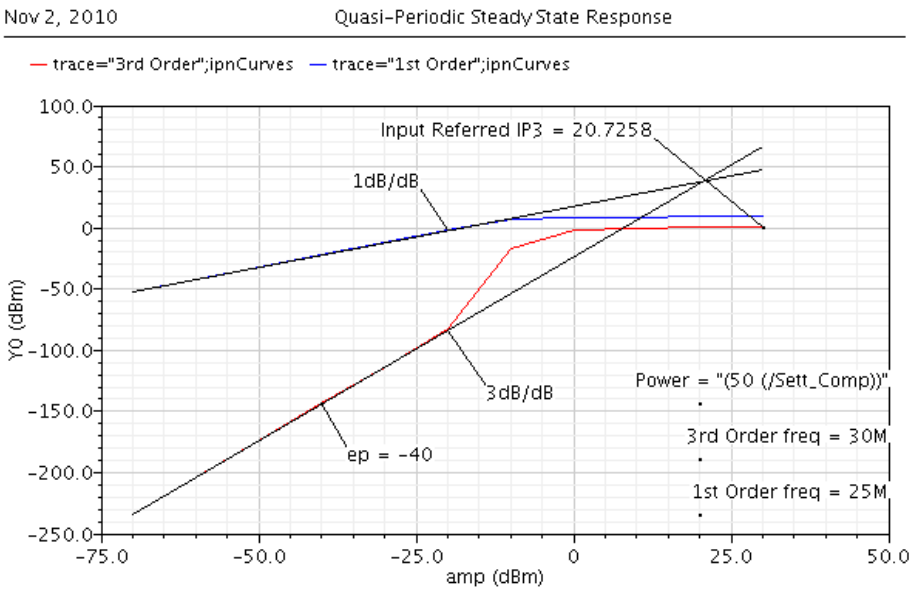

Figure 25: IIP_3 simulation

EIRNV: The spotnoise value is determined at 20MHz, being located outside the flickernoise corner (5MHz), for preventing flickernoise contributions as much as possible. The noise simulation is performed with a PSS & periodic noise (PNOISE) analysis. In PSS the maximum alternating current frequency (maxacfreq) parameter is set to 11GHz and in PNOISE the reference side-band (RSB) parameter to 0 and the maximum side-band (MSB) parameter to 50. This way no frequency conversion is considered and the accuracy due to noise folding will be within 2% [16]. The simulation result is shown in {Figure 26} for a beatfrequency of 20MHz. The derived EIRNV value of 3.2nV/√Hz proofs almost adequate {1.1.2}.

Device	Param	Noise Contribution	% Of Total
I332.I506._1PT_l.m1	Sth	4.23341e-09	16.57
I332.I506._1PT_r.m1	Sth	4.23341e-09	16.57
I332.I506._1NB_l.m1	Sth	3.4034e-09	10.71
I332.I506._1NB_r.m1	Sth	3.4034e-09	10.71
I332.I506._1IN_r.m1	Sth	2.96858e-09	8.15
I332.I506._1IN_l.m1	Sth	2.96858e-09	8.15
I332.I506._1NB_l.m1	Sfl	1.23507e-09	1.41
I332.I506._1NB_r.m1	Sfl	1.23507e-09	1.41
I332.I506._1IN_l.m1	Sfl	1.12719e-09	1.17
I332.I506._1IN_r.m1	Sfl	1.12719e-09	1.17
I332.I506._1PT_l.m1	Sfl	9.25681e-10	0.79
I332.I506._1PT_r.m1	Sfl	9.25681e-10	0.79

Spot Noise Summary (in V/sqrt(Hz)) at 20M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.03992e-08
Total Input Referred Noise = 3.19163e-09
The above noise summary info is for pnoise data

Figure 26: EIRNV simulation

A_{CL} and BW_{CL}: The closed loop- gain and bandwidth are determined with PSS & periodic alternating current (PAC) analysis. The beat frequency is set at 200MHz since the clock frequency is now the only frequency present in the circuit. The RSB parameter was again set at 0 for direct frequency conversion. The results displayed in {Figure 27} show a A_{CL} of ~12dB and a BW_{CL} of ~ 87MHz. Again adequate {1.1.2}.

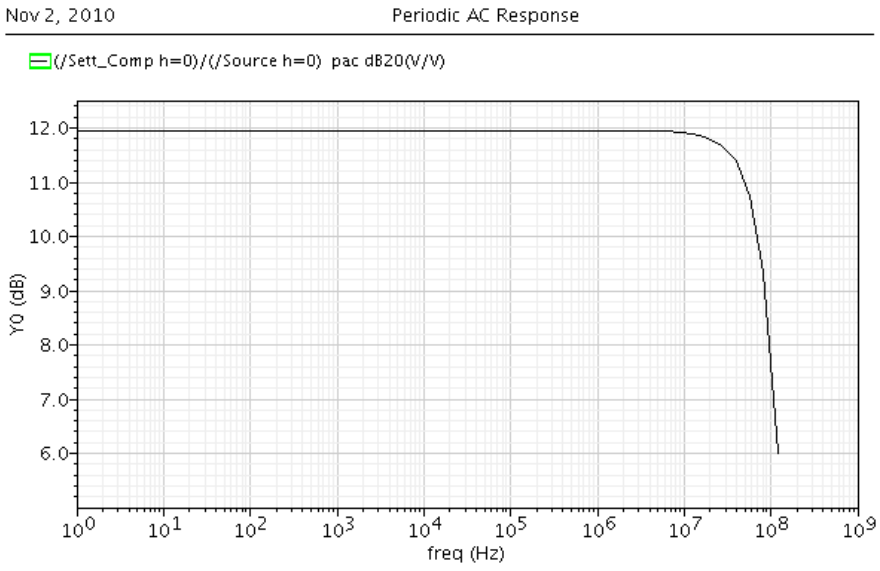

Figure 27: A_{CL} and BW_{CL} simulation

Power: The power dissipation of the circuit is determined by multiplying the supply-voltage with the current and equals 14.6mW. This value can be downscaled, without effecting other design parameters, by downscaling the power dissipation in the SC-CMFB current mirror to an aducuately low level regarding {1.1.2}.

{Table 4} summarizes the performance results for a quick comparison.

	Desired	Obtained
IIP_3 [dBm]	*≥20*	*20.7*
EIRNV [nV/√Hz]	*≤3*	*3.2*
A_{CL} [dB]	*≥12*	*~12*
BW_{CL} [MHz]	*≥25*	*87*
Power [mW]	*≤10*	*14.6*

Table 4: Desired and obtained performance

2.5 Summary:

A fully differential feedback amplifier is proposed for high $IMFDR_3$ with capacitive feedback favored over resistive feedback regarding proper mixer interfacing. This eventually resulted into a discrete-time operated switched-capacitor amplifier design. Inside the feedback network a two-stage folded cascode Miller Op Amp is used with common source output stage for high linearity performance. The amplifier design is nonetheless still basic since large parts are ideal or even completely omitting. Proper circuit functionality and -performance is verified giving enough confidence to proceed with chapter {3}.

3 SC-FDA *analysis* for high IMFDR$_3$:

The aim of this project is the design of a high IMFDR$_3$ amplifier with proper mixer interfacing. Having determined the basic amplifier topology in chapter {2}, the biasing- and dimensioning effects upon high IMFDR$_3$ are analyzed in this chapter for CMOS 65nm technology. From the research conducted design advices will be derived to propose a final design in chapter {4} ultimately.

3.1 Introduction:

In this chapter the basic amplifier topology is analyzed for high IMFDR$_3$. Doing so the feedback network {3.2} and the Op Amp {3.3} are both subjected to linearity- and noise simulations. The feedback network draws first interest since it's realized with ideal components and hence only the dimensioning is considered. First the capacitor ratio will be determined {3.2.1} followed by the absolute dimensioning {3.2.2}. Regarding the Op Amp first the distortion- and noise locations will be pinpointed, followed by biasing- and dimensioning suggestions for optimization {3.3}. In paragraph {3.4} a brief summary is given before proceeding with the final design in chapter {5}. During all simulations the clock frequency is held at 200MHz with 50% dutycycle (two-phase operation) and proper circuit operation is verified {2.4.1}.

3.2 High IMFDR$_3$ feedback network:

Due to the ideal feedback network implementation no biasing dependencies exist and only the dimensioning is addressed. This is discussed in this paragraph.

3.2.1 Relative dimensioning: In this section the influence of the closed-loop gain value upon the linearity- and noise performance is analyzed to determine the feedback capacitor ratio. Lower closed-loop gain values are expected to result into higher linearity performance due to larger loopgain values while not influencing the amplifier noise performance {1.2.4}. The feedback network capacitors won't contribute noise themselves being ideal components with infinite quality factors and hence negligible small equivalent series resistance.

The theory is now verified and quantified with circuit simulations. From the specifications {1.1.2} the closed-loop gain value should be chosen ≥ 4 and hence C_1/C_2 neglecting the small gain error. For the simulation it is chosen to change the A_{CL} from 4 till 8 by increments of 1. This should visualize the performance trends sufficiently while the loopgain is halved. The feedback network capacitor values are chosen as large as possible. In practical situations this will reduce the channel-charge injection effects, noise and mismatch. Consequently C_1 is fixed at 1pF (maximum mixer loading) while C_2 is varied. The Miller frequency compensation capacitors are fixed values for constant bandwidth while voltage settling is verified for unchanged loading conditions. The effects upon the linearity- and noise performance are displayed in {Figure 28} with the essential/modified component values of {Table 5}. The simulation results confirm the prior theory. Feedback shows strong influence upon the linearity performance while almost no effect upon the noise performance. The conclusion is drawn to design for minimum closed-loop gain value (4×) for having maximum IMFDR$_3$ performance.

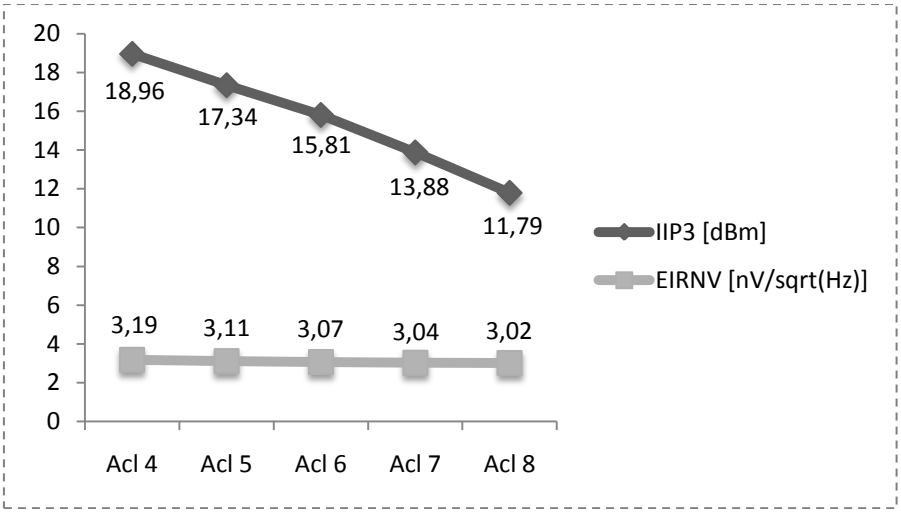

Figure 28: Relative dimensioning behavior

A_{CL}	*4*	*5*	*6*	*7*	*8*
C_1 [fF]	*1000*	*1000*	*1000*	*1000*	*1000*
C_2 [fF]	*250*	*200*	*167*	*143*	*125*
C_C [fF]	*800*	*800*	*800*	*800*	*800*

Table 5: Relative dimensioning values

3.2.2 Absolute dimensioning: In this section the influence of the feedback network capacitors absolute dimensioning upon the linearity- and noise performance is analyzed. Having determined the relative dimensioning in the preceding section {3.2.1} the question still remains whether to implement the obtained closed-loop gain value with either large- or small feedback network capacitor sizes. Keeping the closed-loop gain value constant (4×) the loopgain is kept constant and the linearity should remain constant {1.2.4}. The noise contribution should also remain constant because feedback has no effect upon the noise performance {1.2.4} when the feedback network is noiseless.

The above theory is now verified and quantified with circuit simulations. From the relative dimensioning {3.2.1} the closed-loop gain value is set equal to 4× for high $IMFDR_3$. Additionally it was chosen to decrease C_1 from 1000fF (maximum mixer loading) till 200fF with 200fF steps (5 data points) while changing C_2 accordingly to keep the closed-loop gain value equal to 4×. This approach should visualize the performance trends sufficiently while large part of the allowed feedback network capacitor sizes is covered. The Miller frequency compensation capacitors are fixed for constant bandwidth while voltage settling is verified for unchanged loading conditions. The effects upon the linearity- and noise performance are displayed in {Figure 29} with the essential/modified component values stated in {Table 6}.

The simulation results confirm the prior theory for a large range of feedback network capacitor sizes except for the smallest ones. Since smaller feedback network capacitor sizes require smaller Miller frequency compensation capacitors, the problem may be explained with an overdamped response resulting into insufficient voltage settling. The according gain reduction will then show linearity reduction and noise increase as shown. Nevertheless the conclusion is drawn to use maximum feedback network capacitor values for maximum $IMFDR_3$ performance in realistic- rather than ideal feedback network implementations.

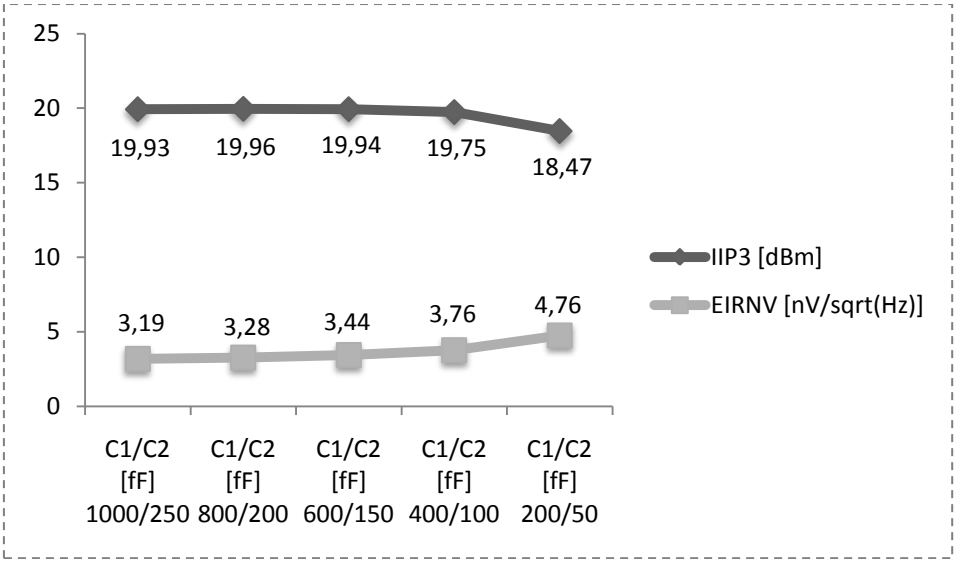

Figure 29: Absolute dimensioning behaviour

A_{CL}	*4*	*4*	*4*	*4*	*4*
C_1 [fF]	*1000*	*800*	*600*	*400*	*200*
C_2 [fF]	*250*	*200*	*150*	*100*	*50*
C_C [fF]	*900*	*900*	*900*	*900*	*900*

Table 6: Absolute dimensioning values

In this paragraph the amplifier feedback network was analyzed for high $IMFDR_3$ demanding large- relative- and absolute dimensioning of the feedback network capacitors. These settings are used for the upcomming high $IMFDR_3$ Op Amp analysis.

3.3 High $IMFDR_3$ Op Amp:

With the feedback network analyzed the focus is redirected towards the Op Amp. The Op Amp noise- and distortion locations will be determined together with biasing- and dimensioning considerations for $IMFDR_3$ optimization.

3.3.1 Noise location: In this section the major noise location within the amplifier Op Amp is determined for allowing later noise optimizations {3.3.2}. Since feedback ideally doesn't influence the amplifier noise performance {1.2.4}, the Friis theory for open-loop cascaded circuits is considered. According to this theory the (linearity and) noise of subsequent stages is downscaled by the gain of preceding stages. Recognizing the Op Amp input stage as high gain stage (common for Op Amps) and the Op Amp output stage as having few noisy components the folded cascode input stage is expected to be the dominant noise contributor.

The above theory is verified and quantified with the circuit noise simulation displayed in {Figure 26} before.

The 'noise summary' simulation confirms the prior theory. The noise dominantly origins from (MOST devices located in) the input stage. Hence the conclusion is drawn to optimize the input stage for low noise in an attempt to design a high $IMFDR_3$ amplifier. This topic is discussed in the next section.

3.3.2 Low noise input stage design: From {Figure 26} it is determined to focus attention upon the thermal noise contribution (Sth) being the largest noise contributor. The flicker noise (Sfl) contribution is easily ignored, considering the design of an IF-amplifier, while flickernoise resides at baseband.

Biasing: Regarding the thermal noise contribution of the folded cascode input stage the following equation is found [1].

$$\overline{V_N{}^2,_{IN}} = 8kT\left(\frac{2}{3gm_{1IN}} + \frac{2gm_{1PT}}{3gm^2{}_{1IN}} + \frac{2gm_{1NB}}{3gm^2{}_{1IN}}\right) \tag{3.1}$$

In the above equation two possible ways to decrease the noise are indicated considering the temperature as an uncontrolled variable. The first way is to decrease the transconductance of the current source MOSTs and the second way is to increase the transconductance of the signal MOSTs. Although being the smallest thermal noise contributors in {Figure 26} the transconductance of the signal MOSTs is expected to be the dominant factor in improving the noise performance of the amplifier. This due to the mathematical power dependence and being mentioned in each individual term in the above equation. Further the equation indicates no noise dependency upon the tail current source- and the cascode devices which again is verified in {Figure 26}. The noise from the tail current source is injected into both signal paths resulting as a common-mode rather than a differential-mode noise component. The noise currents from the four cascode devices are effectively shorted and are not flowing out of these devices [1]. Also regarding the SC-CMFB network no noise contribution is seen. The sensing capacitors are ideal components while the voltage biasing MOST is disconnected during the amplification phase. The MOST transconductance can be expressed as shown in the equation below [1] indicating complete noise dependency upon the biasing conditions. All this will be verified here to be complete regarding the Op Amp input stage design.

$$gm = \frac{2Id}{Vgs - Vth} = \frac{2Id}{Vgt} \tag{3.2}$$

The theory is now verified and quantified with circuit simulations. From {Figure 26} it is determined that indeed the current source- and signal MOSTs are the noise contributors of the amplifier input stage. Now the gate-source voltage (V_{GS}) for these devices is swept individually, while remaining biased in saturation region, over a broad range to visualize the noise performance trends. Sweeping the drain current (I_D) will effect multiple MOSTs and therefore isn't considered. The MOST width is adapted for not changing the biasing conditions. The Miller frequency compensation capacitors are fixed for constant bandwidth while voltage settling is verified for unchanged loading conditions. The effect of transconductance changes for the signal- and current source MOST devices upon the noise performance are displayed in {Figure 30}, {Figure 31} and {Figure 32} with the essential/modified component values mentioned in {Table 7}, {Table 8} and {Table 9} respectively.

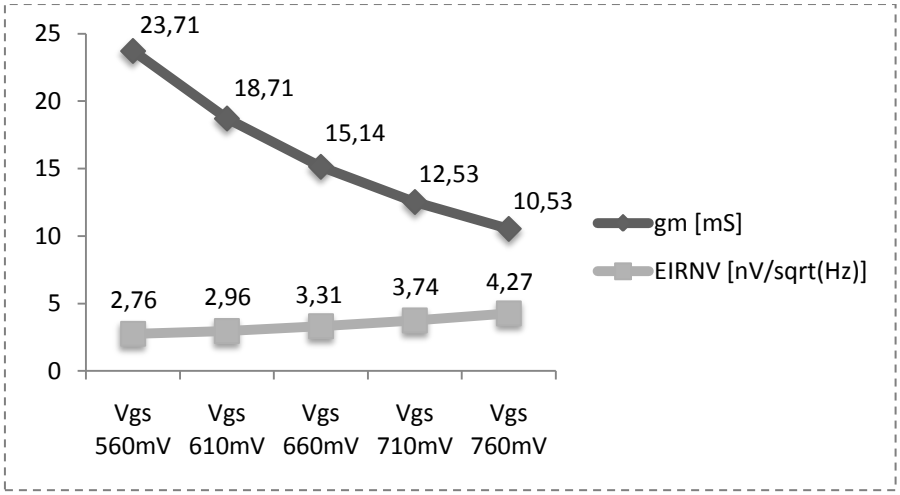

Figure 30: Input NMOST behaviour

Vgs [mV]	*560*	*610*	*660*	*710*	*760*
W [μm]	*233.0*	*115.4*	*65.9*	*41.6*	*28.4*
rds [Ω]	*891*	*1011*	*1121*	*1217*	*1300*

Table 7: Input NMOST values

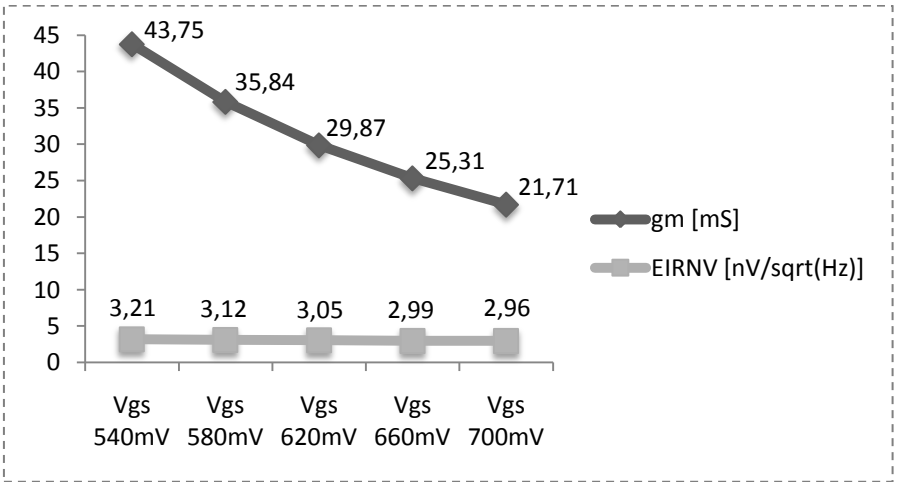

Figure 31: PMOST Isrc behaviour

Vgs [mV]	*540*	*580*	*620*	*660*	*700*
W [μm]	*1118*	*659.4*	*426.3*	*295.5*	*216.1*
rds [Ω]	*431*	*444*	*454*	*460*	*459*

Table 8: PMOST Isrc values

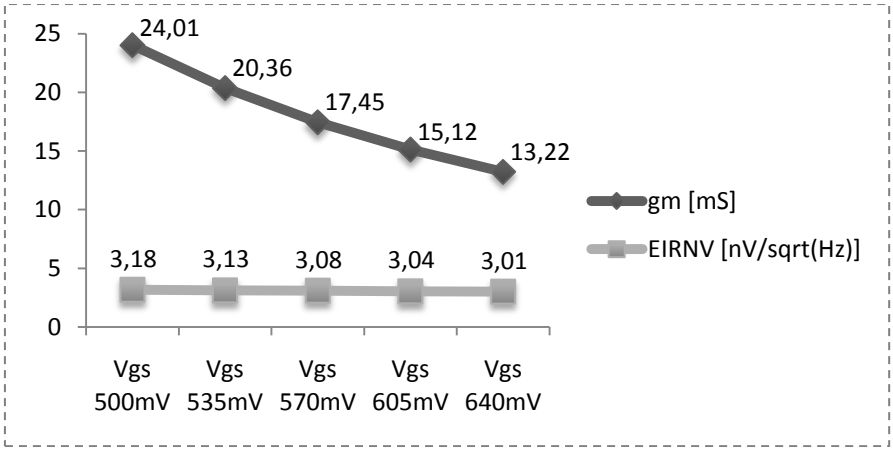

Figure 32: NMOST Isrc behaviour

Vgs [mV]	*500*	*535*	*570*	*605*	*640*
W [μm]	*256.6*	*153.2*	*98.7*	*67.5*	*48.6*
rds [Ω]	*730*	*778*	*821*	*857*	*881*

Table 9: NMOST Isrc values

The simulation results displayed in {Figure 30}, {Figure 31} and {Figure 32} confirm the prior theory. The transconductance of the signal MOSTs have strong influence upon the noise performance and should preferable be maximized. The transconductance of the current source MOSTs have weak influence upon the noise performance and should preferable be minimized. Regarding the signal MOSTs the bandwidth is increased for larger transconductance values, increasing the noise bandwidth and hence the noiselevel, counteracting the lower obtained spotnoise value. Regarding the current source MOSTs, lowering the transconductance value will increase the drain-source saturation voltage, which potentially increases the distortion from the cascode devices due to weaker voltage biasing [5], {3.3.4}. Regarding input stage biasing for low noise the signal MOST voltage biasing should be minimized.

Dimensioning: With the biasing dependencies determined the circuit dimensioning is limited to integer upscaling of the MOSTs- widths and lengths together as shown in the equation below. This integer upscaling means that the actual MOST length is always chosen an integer multiple of the minimum MOST length (for layout considerations) and that this integer length multiplication factor must be applied to the MOST width as well to keep the current biasing constant.

$$Id = \frac{1}{2}\mu nCox\frac{W}{L}(Vgs - Vth)^2 \qquad (3.3)$$

Although maintaining a constant MOST width-to-length ratio integer upscaling increases the MOST output impedance due to less channel length modulation [1]. Due to the increased output impedance the input stage gain can be increased and the noise decreased as known from the Friis theory of cascaded circuits. However the previous noise equation doesn't mention MOST output impedances and hence better noise performance isn't expected. Multiplying the MOST noise currents with $(R_{OUT1})^2$ towards the input stage output and then dividing with $(gm_{1IN}\times R_{OUT1})^2$ towards the input stage input, this term is effectively factored out.

The theory is now verified and quantified with circuit simulations. To increase the gain of the input stage effectively the weak output impedance of the current source PMOST device is increased by integer upscaling. The PMOST length is swept from 0.18um in five successive steps (determined by the minimum transistor length) to 0.42um to cover a realistic device length range for visualizing the noise performance trend. For each different length a different width is assigned for not altering the biasing conditions. The Miller frequency compensation capacitors are fixed for constant bandwith while voltage settling is verified for unchanged loading conditions. The effect of input stage gain changes upon the noise performance is shown in {Figure 33} with the essential/modified component values given in {Table 10}.

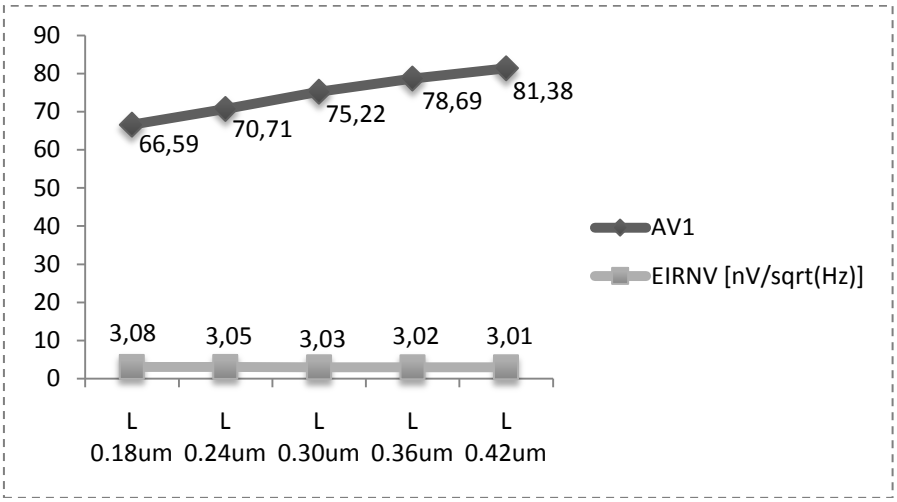

Figure 33: PMOST Isrc behaviour

W [μm]	*525*	*629.3*	*710.5*	*798.3*	*889.3*
L [μm]	*0.18*	*0.24*	*0.30*	*0.36*	*0.42*
rds [Ω]	*449*	*510*	*584*	*650*	*706*

Table 10: PMOST Isrc values

The simulation results displayed in {Figure 33} confirm the prior theory. Increasing the gain of the input stage is shown to have negligible effect upon the amplifier (input stage) noise performance. Regarding input stage dimensioning for low noise no dependency is concluded to exist when limited by integer upscaling.

3.3.3 Distortion location: In this section the major distortion location within the amplifier Op Amp is determined for allowing later distortion optimization in section {3.3.4}. Loopgain is well known to result into distortion suppression while creating a virtual ground node at the Op Amp input terminals. Hence distortion suppression is linked with signal swing reduction. For an amplifier clearly the largest signal swings are in the output stage, expecting this stage to be the largest distortion contributor. This is also generally expected from the Friis theory of cascaded circuits although this theory applies for open-loop cascaded stages.

The above theory is now verified and quantified with circuit simulation. Practically no distortion contribution from the CMFB networks is considered when the common-mode UGF is ≥ the differential-mode UGF [14]. Here no distortion contribution is assumed since the CMFB networks are ideal and based upon voltage settling. Hence the focus is directed towards the remaining Op Amp MOSTs. To determine the individual MOSTs distortion contribution the signal swings obtained with SpectreRF are applied in ProMOST. For proper comparison the swings are determined in a fixed amplification phase when being settled to neglect the settling behaviour. The sinusoidal input signal applied is assigned an amplitude of -40dBm with a frequency of 20MHz. The amplitude chosen operates the circuit in weak nonlinear region to prevent saturation effects to be accounted for. The frequency can be chosen quite arbitrary, since this doesn't effect the relation between the MOSTs swings, due to the discrete-time operation of the circuit. For continuous-time operated circuits the relative distortion contributions between the MOSTs in the input-and output stage decrease as a function of the input signal frequency. Since the input stage has a low frequency pole (and the output stage a high frequency pole) the gain of the input stage will drop earlier during input signal frequency increase. This input stage gain reduction will increae the swings in the input stage explaining the situation. Since the Op Amp tail current source- and the SC-CMFB bias voltage MOST are situated outside the differential-mode signal path these devices aren't producing any distortion and hence are ignored. The obtained MOSTs distortion contributions are displayed in {Figure 34}.

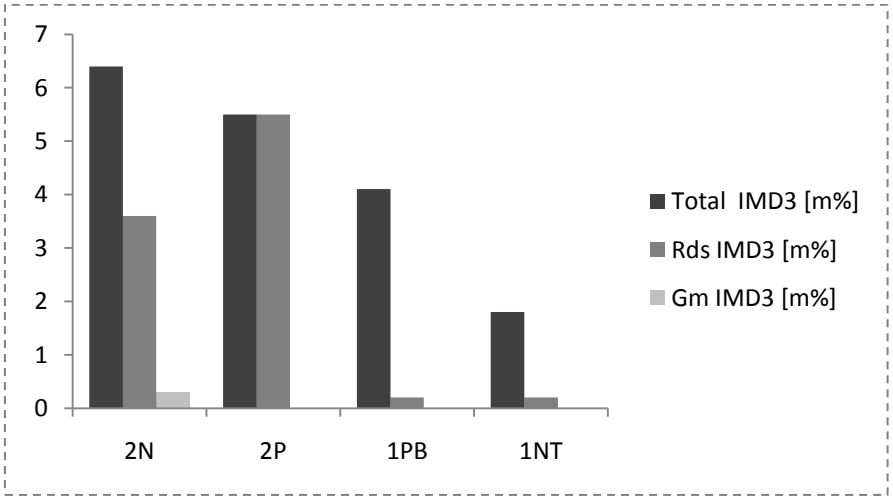

Figure 34: MOSTs IMD_3 contribution

{Figure 34} confirms the prior theory. The output stage MOSTs show the largest distortion contribution (Total IMD_3 [m%]) and hence the output stage is considered the major distortion contributor. The summed distortion contribution from the remaining not mentioned MOSTs was negligible, probably due to the very small voltage swings and is hence left out of {Figure 34}. To optimize the Op Amp and hence the amplifier for low distortion it is concluded to optimize the output stage (and to a lesser extend also the input stage cascode devices at the stages interface) for low distortion. This is discussed in the next section.

3.3.4 Low distortion output stage design: Although the main goal is still to design a high $IMFDR_3$ amplifier with proper mixer interfacing an additional research question to identify the dominant distortion mechanism. Recognizing the output stage signal MOST (2N) as the dominant distortion contributor {Figure 34} further analysis is conducted upon this component. For determining the dominant distortion mechanism use is made of the MOST small-signal model [1] given in {Figure 35}.

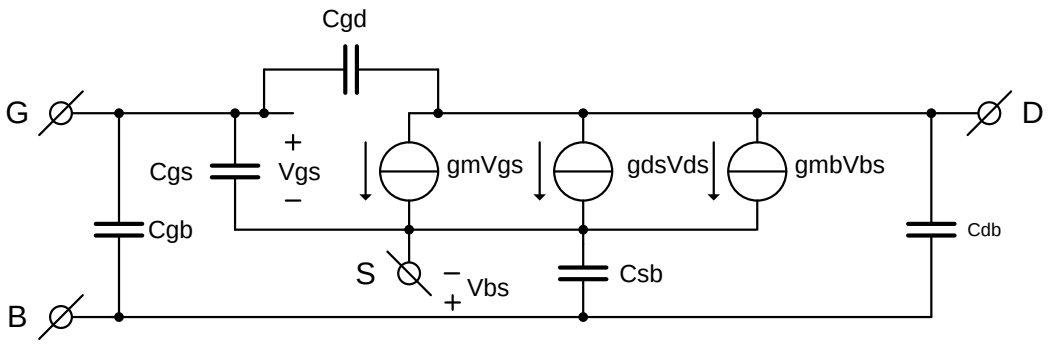

Figure 35: General MOST small-signal model

Knowing that the MOST capacitances only contribute distortion at high- frequency and swing nodes [5] no distortion contribution is expected considering the voltage settling based amplifier operation. Additionally no distortion due to body-effect (g_{mb}) is considered since the bulk- and source contacts are shorted. Due to terminal voltage excitation nonlinear currents start flowing emphasizing the voltage swing dependency of distortion. Therefore the only remaining distortion mechanisms are the MOSTs-transconductance and output impedance reducing {Figure 35} into {Figure 36}.

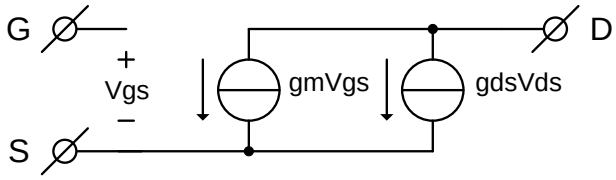

Figure 36: Output stage MOST small-signal model for distortion

Although the MOST small-signal model is strongly reduced determining the dominant distortion mechanism is still difficult. Generally the largest nonlinear coefficients are expected for the MOST transconductance knowing the squared drain current dependence upon the gate-source voltage. Channel-length modulation creating output impedance distortion is often considered a second-order effect. However due to amplification the MOST signal swings at the output are generally higher than at the input indicating the output impedance as the potential dominant distortion mechanism. The determination of the dominant distortion mechanism is verified and quantified in {Figure 34}.

From the simulation results displayed the MOST transconductance distortion contribution is ignored indicating the MOST output impedance as the dominant distortion mechanism. However since the output impedance distortion contribution is less than the total distortion contribution additional large distortion contribution is expected from the transconductance and output impedance crossproducts.

Biasing: Regarding MOST biasing for low IMD_3 only the effect of changing gate-source voltages for the output stage signal MOSTs (2N) are considered. Based upon the relative current swing parameter [9] the distortion is expected to decrease linearly with increasing power. Hence distortion simulations for changing current biasing conditions are redundant. Additionally the drain-source biasing isn't considered since potential biasing improvements for the signal MOST are expected to deteriorate those for the current source MOST (2P) being directly connected. In general assuming similar biasing dependencies for signal- and current source MOSTs is not assumed [5] but nevertheless done here expecting similar underlying distortion mechanism. Now for low gate-source voltages the nonlinear coefficients associated with the transconductance will be assumed high and for high gate-source voltages the nonlinear coefficients associated with the output impedance [5]. Knowing that the MOST- output impedance contribute more distortion than than the transconductance {Figure 34} applying minimum gate-source biasing is assumed beneficial for low IMD_3.

The above theory is now verified and quantified with IMD_3 simulations. The gate-source voltage is swept through saturation region while keeping the biasing current fixed demanding MOST width modification. The effect of gate-source voltage modification upon the IMD_3 performance is displayed in {Figure 37} with the essential/modified component values stated in {Figure 11}.

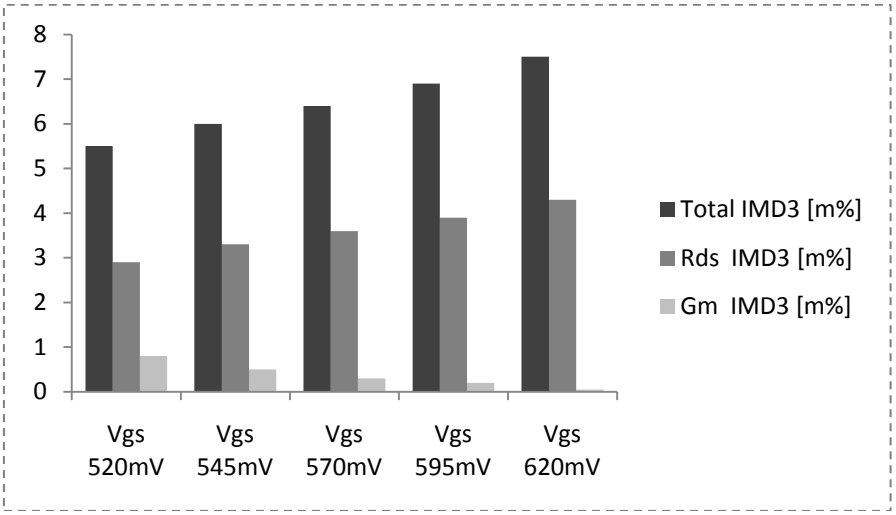

Figure 37: IMD3 versus Vgs simulation

Vgs [mV]	*520*	*545*	*570*	*595*	*620*
W [um]	*152.5*	*109.4*	*81.27*	*62.17*	*48.79*

Table 11: IMD3 versus Vgs values

The simulation results displayed in {Figure 37} confirm the prior theory. Weak gate-source voltage biasing renders low MOST total- and rds IMD_3 with high gm IMD_3 while the opposite is true for high gate-source voltage biasing.

The conclusion is drawn that the distortion generating MOSTs in {Figure 34} should preferably be biased with low gate-source voltage biasing.

Dimensioning: Regarding MOST dimensioning for low IMD3 only the effect of integer upscaling for the output stage signal MOST (2N) is considered. Similar dimensioning dependencies for signal- and current source MOSTs are assumed expecting similar underlying distortion mechanisms. With the biasing conditions previously determined the circuit dimensioning is limited to integer upscaling of the MOSTs- widths and lengths. The main effect of integer upscaling is higher MOST output impedance due to less channel length modulation. Since integer upscaling doesn't effect the MOST transconductance only the nonlinear coefficients associated with the output impedance are expected to change. For longer MOSTs the affect of channel length modulation reduces expecting to result into lower IMD_3 values. Knowing that the MOST- output impedance contributes more distortion than the transconductance {Figure 34} applying maximum dimensioning is assumed beneficial for low IMD_3.

The above theory is now verified and quantified with IMD_3 simulations. The MOST length is swept from 0.06um in five successive steps (determined by the minimum MOST length) to 0.30um for visualizing the IMD_3 performance trend. For each different length a different width is assigned to keep the biasing conditions fixed. The effect of MOST integer upscaling upon the IMD_3 performance is displayed in {Figure 38} with the essential/modified component values stated in {Table 12}.

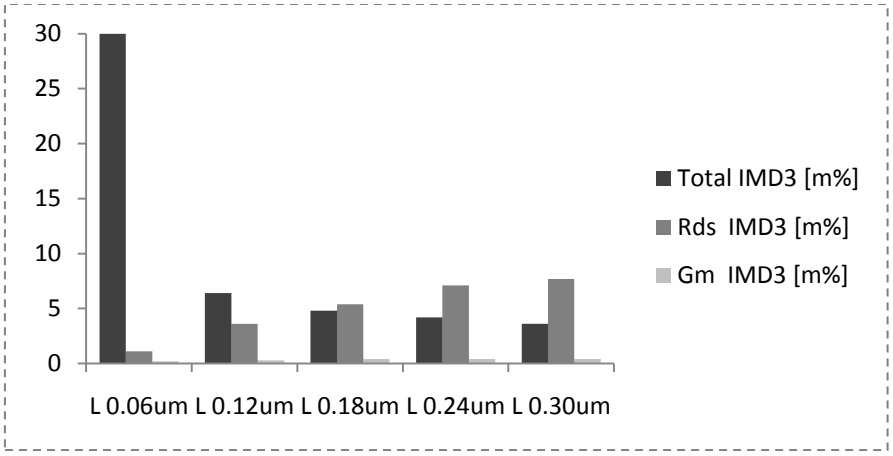

Figure 38: IMD3 versus dimensioning simulation

W [μm]	*41.64*	*81.27*	*116.9*	*150.4*	*167.9*
L [μm]	*0.06*	*0.12*	*0.18*	*0.24*	*0.30*

Table 12: IMD3 versus dimensioning values

The simulation results displayed in {Figure 38} confirm the prior theory partly. Larger MOST dimensioning is indeed showing lower total IMD_3 while the gm IMD_3 remains relatively constant. Awkward to explain is the rds IMD_3 increase for larger dimensioning while the opposite is expected due to lower channel length modulation. Nevertheless the conclusion is drawn that the MOSTs generating distortion {Figure 34} should preferably have large dimensioning for low IMD_3.

3.4 Summary:

In this chapter distortion- and noise simulations are conducted to be able to design a SC-FDA for high $IMFDR_3$ ultimately. In essence the research reveals biasing- and dimensioning considerations for proper design. For the ideal feedback network no biasing dependencies exist and only the dimensioning is considered. The feedback network dimensioning is found to have very strong effect upon the amplifier linearity performance. For this the feedback factor value should be chosen as large as possible for realizing maximum loopgain, resulting into small- signal swings and hence distortion. Additionally the feedback network capacitor sizes should be chosen large based upon expected practical considerations. Regarding the Op Amp the input stage is the major noise contributor and the output stage the major distortion contributor. This was already tacitly assumed from the Friis theory of cascaded circuits although this theory essentially applies for open-loop situations. In the input stage the thermal noise is the major noise contributor, considering an IF-amplifier, while flickernoise resides at baseband. The thermal noise contribution is dominantly determined by the biasing conditions of the input stage signal MOSTs for which the transconductance should be maximized. Integer upscaling of the MOSTs in the input stage is shown to have negligible effect. In the output stage the main distortion contributing mechanisms are the MOST- output impedance and crossproducts of the output impedance and transconductance. To lower the MOST total IMD_3 the gate-source biasing should be minimized while the dimensioning is maximized. Remarkable and unexplained is the increase in MOST output impedance IMD_3 for increasing dimensioning while the opposite was expected considering smaller channel length modulation.

4 SC-FDA *design* for high IMFDR$_3$:

The aim of this project is the design of a high IMFDR$_3$ amplifier with proper mixer interfacing. In this chapter the analysis results from chapter {3} are applied upon the basic amplifier topology proposed in chapter {2}. This will result in the final design for high IMFDR$_3$ as initially requested.

4.1 Introduction:

In this chapter the basic amplifier topology is designed for high IMFDR$_3$. The design steps are discussed first {4.2.1} after which the circuit is simulated to determine the final specifications {4.2.2}. Comparing the final specifications with those initial stated will be done subsequently {Table 13} to determine if further circuit tweaking is demanded. In the last paragraph of this chapter {4.3} a brief summary will be given before proceeding with the conclusions and recommendations in chapter {5}.

4.2 Final design:

4.2.1 Design conditions: From the clock frequency, closed-loop gain and system resolution it is possible to determine the minimum desired UGF- and loopgain value. Knowing these two parameters the final design of the circuit is determined regarding, IMFDR$_3$ research results, slew-free operation, meeting design specifications and realizing stable circuit operation all at once. This line of reasoning is discussed upon below starting with the clock frequency.

Fclk: To couple the amplifier directly to the preceding mixer stage they should both be operated at the same clock frequency. The mixer clock frequency operation range was determined from 200MHz till 2GHz [7]. Generally the circuit speed trades with the circuit gain which is well known to result into higher linearity performance being the dominant design consideration. The design for minimum clock frequency further minimizes the current usage and hence power dissipation. Design for 200MHz clock frequency is hence assumed to outweigh the benefits of high clock frequency operation like less aliasing and larger time resolution.

Acl: The closed-loop gain value is chosen minimum for maximum IMFDR$_3$ performance {3.2.1} and according to the specifications {1.1.2} this value equals 4. A potential disadvantage of a smaller closed-loop gain is a higher loopgain and hence worse circuit stability. However due to the low clock frequency a large frequency compensation capacitor is allowed to still result into stable circuit operation. Additionally the feedback network capacitors should be chosen maximum for maximum IMFDR$_3$ performance in practical situations {3.2.2}. The maximum feedback network input capacitor value is determined 1pF for not loading the previous mixer circuit too much. Now to realize the closed-loop gain value of 4 times the feedback network output capacitor value was chosen 250fF.

UGF: Relating the amplifier unity gain frequency with the ampifier dominant pole location it determines the transient signal response at the circuit output. It should be understood that the mimimum desired unity gain frequency depends on the dynamic settling accuracy and the closed-loop gain value that must be provided [1].

$$\tau \approx \frac{A_{CL}}{UGF} \tag{4.1}$$

The settling accuracy relates to the total settling error as indicated below.

$$accuracy = 1 - error \tag{4.2}$$

The total settling error is composed of two components, the static settling error and the dynamic settling error. The static settling error relates to finite loopgain whereas the dynamic settling error relates to finite UGF. According to [6] the total settling error should be ≤ LSB/2 for preventing missing codes. Hence it is assumed that both the static settling error and the dynamic settling error should each be ≤ LSB/4 to fulfil the requirement. The dynamic settling error can be further decomposed in slewing error and linear settling error. Slewing error can and will be prevented for by proper circuit current- and voltage biasing as can be read later. The remaining linear settling error relates to the natural response of a circuit, which for a first-order system is given below.

$$V_{OUT}(t) \approx V_{OUT,FINAL}\ \ 1 - \exp^{-t/\tau} \tag{4.3}$$

Assuming a 10-bit system resolution the maximum allowed linear settling error becomes

$$\begin{gathered} 10 - bit\ resolution = 2^{\wedge 10} = 1024\ steps \\ LSB/4 \approx 2.5 \times 10^{-4} \end{gathered} \tag{4.4}$$

Now the maximum allowed time constant can be determined from above.

$$\begin{gathered} \exp^{-t/\tau} \leq 2.5 \times 10^{-4} \\ \tau \leq 300\,ps \end{gathered} \tag{4.5}$$

Regarding equation {4.1} the UGF value should be chosen ≥ 13.33Grad/sec for a closed-loop gain value of 4 times to realize the desired settling accuracy. From equation {2.5}design for minimum UGF is assumed to give enhanced circuit stability allowing larger frequency compensation capacitors usage. Aiming at a common transconductance value of 20mS for the input MOSTs the maximum on-chip frequency compensation capacitor value is determined at 1.5pF.

Loopgain: The required loopgain depends on the static settling accuracy that must be realized.The feedback factor is indicated in the equation below [1].

$$B = \frac{C_2}{C_1 + C_2 + C_{IN}} = \frac{C_2}{5C_2 + C_{IN}} \tag{4.6}$$

Assuming large Op Amp gain the amplifier closed-loop gain is given [1].

$$\left|\frac{V_{OUT}}{V_{IN}}\right| \approx \frac{C_1}{C_2}\left(1-\frac{C_1+C_2+C_{IN}}{C_2}\frac{1}{A}\right) \approx \frac{C_1}{C_2}\left(1-\frac{1}{AB}\right) \tag{4.7}$$

The above equation shows that larger loopgain results in lower relative gain error and hence lower static settling error. To keep the static settling error below LSB/4 the loopgain should be chosen.

$$AB \geq 4000 \tag{4.8}$$

Considering a realistic feedback factor value of around 6^{-1} the required Op Amp gain becomes 90dB whereas only 60dB is practically realized. A solution to this problem is possibly found by applying switched-capacitor circuits with reduced sensitivity to amplifier gain [11], reducing the Op Amp gain 10-100 times on average. Not knowing the tradeoffs for this technique the Op Amp gain reduction is assumed 50 times reducing the required Op Amp gain till around 55dB. Now an acceptable gain value for the common source output stage is assumed 7 times which requires the folded cascode input stage to realize a gain of 71.5 times.

Voltage biasing: During the discussion of the UGF previously it was mentioned that proper circuit (current- and) voltage biasing should result into slew-free operation. To avoid slewing in the Op Amp the gate voltage of the input transistors should be chosen such that [6].

$$\frac{Vgt}{Vstep} \geq B \tag{4.9}$$

Aiming at a differential rail-to-rail signal swing at the output of the amplifier the maximum single ended signal swing becomes 600mV. With a preferred closed-loop gain value of 4 times, the maximum step signal at the input of the amplifier is 150mV. For a realistic feedback factor value of 6^{-1} this requires an effective gate-source voltage for slew-free operation equal to

$$Vgt \geq \frac{150mV}{6} \geq 25mV \tag{4.10}$$

During the voltage biasing of the Op Amp MOSTs a ±10% deviation in the threshold voltage is considered each time individually. For the input MOSTs this resulted in a minimum and actual Vgt around 50mV meeting the slewing requirement by 2 times. This value is also influencing the power consumption, noise, bandwidth and input stage gain by influencing the transconductance of the input signal MOSTs. Due to the combination of factors a standard transconductance value of 20mS was initially aimed at. The voltage biasing of the output stage signal MOST is chosen minimum for maximum linearity performance {3.3.4}. The remaining MOSTs drain-source voltages are evenly divided by the number of stacked MOSTs. The remaining MOSTs gate-source voltages are placed in the middle of the saturation region. The final result of the voltage biasing for the SC-FDA is shown in appendix {B} (lower values).

Current biasing: During the discussion of the UGF previously it was mentioned that proper circuit (voltage- and) current biasing should result into slew-free operation. To avoid slewing in the Op Amp the slew-rate must be larger than the maximum signal slope in the circuit [6].

$$SR = \frac{I}{C} \geq \left.\frac{dV}{dt}\right|_{\max} \tag{4.11}$$

For an amplifier circuit the maximum dV/dt is expected in the output stage.

Output stage: According to the above equation the minimum bias current for slew-free operation can be determined from multiplication of the output stage node capacitance with the maximum output stage dV/dt. The output stage node capacitance is approximately determined below.

$$C_{OUT2} \approx 0.5C_L + C_C + C_2 + C_{PAR} \approx 0.5\,pF + 1.5\,pF + 0.25\,pF + 0.75\,pF \approx 3\,pF \tag{4.12}$$

Aiming at a differential rail-to-rail signal swing at the output of the amplifier the maximum single ended signal swing becomes 600mV. This value should be achieved in a clock phase settling time of 2.5ns during worst-case operation. Knowing that the settling time equals 5τ and that 64% of the final value is achieved at 1τ the minimum output stage bias current for slew-free operation is determined.

$$I \geq C_{OUT2}\frac{dV}{dt} \geq 3\,pF \times \frac{384mV}{0.5ns} \geq 2.3mA \tag{4.13}$$

Input stage: With a power budget of 10mW and a supply voltage of 1.2V the total bias current available is 8.33mA. Subtracting 4.6mA for slew-free current biasing of the output stage leaves 3.7mA for the slew-free current biasing of the input stage. In the input stage the current biasing of the tail current source is chosen equal to the current biasing of the PMOST current source device [1]. This prevents systematic offset, clamping MOSTs usage and realizes equal positive- and negative slew rates. Effectively four equal current branches are now created, two input current branches and two cascode current branches. With 3.7mA and four equal current branches each branch is assigned a value of 0.93mA. However desiring a standard transconductance value of 20mS for the input signal MOSTs the current branches should be 1.1mA. This will increase the power dissipation from 10mW till around 11mW which is taken for granted. In a similar fashion as for the output stage we can now determine the maximum allowed node capacitance for slew-free operation in the input stage. Remember that the maximum voltage swing is reduced by the gain of the second stage.

$$C_{OUT1} \leq \frac{I}{\frac{dV}{dt}} \leq \frac{1.1mA}{\frac{55mV}{0.5ns}} \leq 10\,pF \tag{4.14}$$

During slewing Miller-effect is ignored [1] and hence satisfying the above equation is reasonably expected. The final result of the current biasing for the SC-FDA is shown along with the voltage biasing in appendix {B} (lower values)

Dimensioning: Having determined the initial biasing conditions the initial dimensioning conditions are still to be discussed which is done below.

Output stage: Considering a MOST intrinsic gain of 20 times an estimated initial gain value for the common source output stage becomes 7 times. Recognizing the output stage as the major distortion contributor {3.3.3} using minimum MOST lengths should be prevented {3.3.4}. Hence the output stage MOSTs lengths initially chosen were 2 times minimum at 120nm. The CMFB sensing resistors were chosen 420Ω for realizing the desired gain of 7 times. The MOSTs widths resulted directly from the assigned combination of MOST- biasing conditions and lengths.

Input stage: Recognizing the input stage as the major noise contributor {3.3.1} no dimensioning dependencies are assumed {3.3.2}. Hence the dimensioning of the input stage confirms to general design considerations. From equations {4.8} and {4.10} larger input MOSTs are known to create smaller feedback factor, demanding larger Op Amp gain to satisfy the static settling accuracy. An initial consideration is then to minimize the lengths of the input MOSTs. This however prevents acceptable gain values to be accomplished for due to a small parallel resistor replacement value. Reason is the parallel placement of a small input NMOST impedance with an already small current source PMOST impedance. Hence the initial input NMOST length was chosen 120nm yielding a C_{IN} of 150fF.

$$B = \frac{C_2}{C_1 + C_2 + C_{IN}} = \frac{250\ fF}{1000\ fF + 250\ fF + 150\ fF} = (5.6)^{-1} \tag{4.15}$$

From equation {4.10} the initial loopgain was determined ≥ 4000 times. With the reduced sensitivity feedback network this value could be reduced towards ≥ 80 times. Now with B equal to $(5.6)^{-1}$ and the output stage gain (A_2) equal to 7 the required input stage gain (A_1) value is determined.

$$AB \geq 80$$

$$A \geq 80 \times 5.6 \geq 448 \quad \rightarrow \quad A_1 \geq \frac{A}{A_2} \geq \frac{448}{7} \geq 64 \tag{4.16}$$

With the transconductance of the input signal NMOSTs already determined the output impedance needed of the folded cascode input stage is calculated.

$$R_{OUT1} \geq \frac{A_1}{gm_{1IN}} \geq \frac{64}{20mS} \geq 3200\Omega \tag{4.17}$$

By assigning all MOSTs 120nm lengths the output impedance became 3400Ω realizing an input stage gain value of 68 times. By preventing minimum MOST length usage for the common gate devices distortion is reduced. The value for the sensing capacitors in the SC-CMFB network and the value of the frequency compensation capacitors were based on achieving fast voltage settling. The resulting capacitor values were well below the limits determined by the desired UGF and slew-rate. The final results of the dimensioning for the SC-FDA are shown in appendix {C} (lower values).

4.2.2 Specifications: The design specifications are determined by simulations using the simulation settings previously used in the performance testing section {2.4.2}. At the end of this section the current design specifications will be compared with the desired specifications {1.1.2} as a guideline for further circuit tweaking.

Linearity:

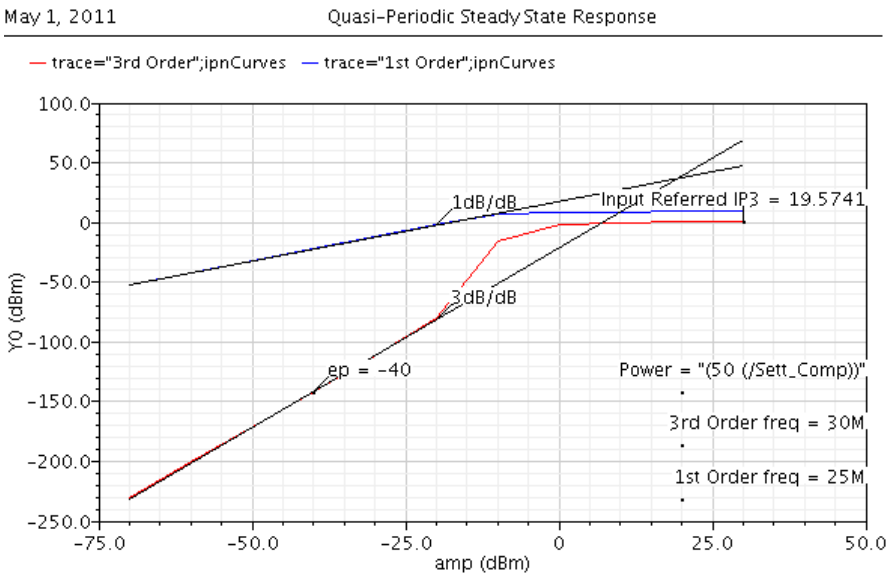

Figure 39: Linearity

EIRNV:

Device	Param	Noise Contribution	% Of Total
I332.I506._1PT_l.m1	Sth	3.52568e-09	12.00
I332.I506._1PT_r.m1	Sth	3.52568e-09	12.00
I332.I506._1NB_l.m1	Sth	3.32984e-09	10.70
I332.I506._1NB_r.m1	Sth	3.32984e-09	10.70
I332.I506._1IN_r.m1	Sth	3.22677e-09	10.05
I332.I506._1IN_l.m1	Sth	3.22677e-09	10.05
I332.I506._1PT_l.m1	Sfl	1.37735e-09	1.83
I332.I506._1PT_r.m1	Sfl	1.37735e-09	1.83
I332.I506._1NB_l.m1	Sfl	1.11911e-09	1.21
I332.I506._1NB_r.m1	Sfl	1.11911e-09	1.21
I332.I506._1PB_l.m1	Sth	8.76271e-10	0.74
I332.I506._1PB_r.m1	Sth	8.76271e-10	0.74
I332.I506._1IN_l.m1	Sfl	7.55989e-10	0.55
I332.I506._1IN_r.m1	Sfl	7.55989e-10	0.55

Spot Noise Summary (in V/sqrt(Hz)) at 20M Hz Sorted By Noise Contributors
Total Summarized Noise = 1.01778e-08
Total Input Referred Noise = 2.93172e-09
The above noise summary info is for pnoise data

Figure 40: Noise

Closed-loop- gain & bandwidth:

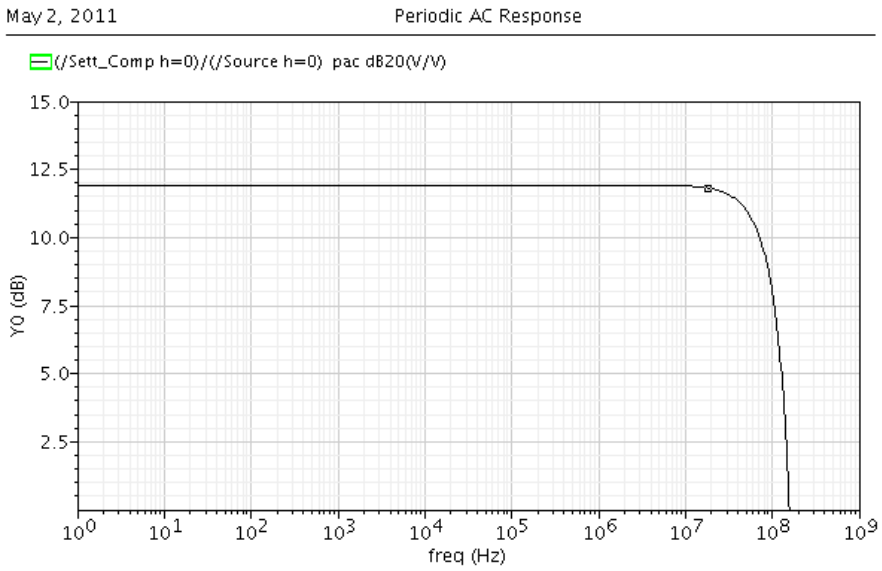

Figure 41: Closed-loop gain- and bandwidth

Power:

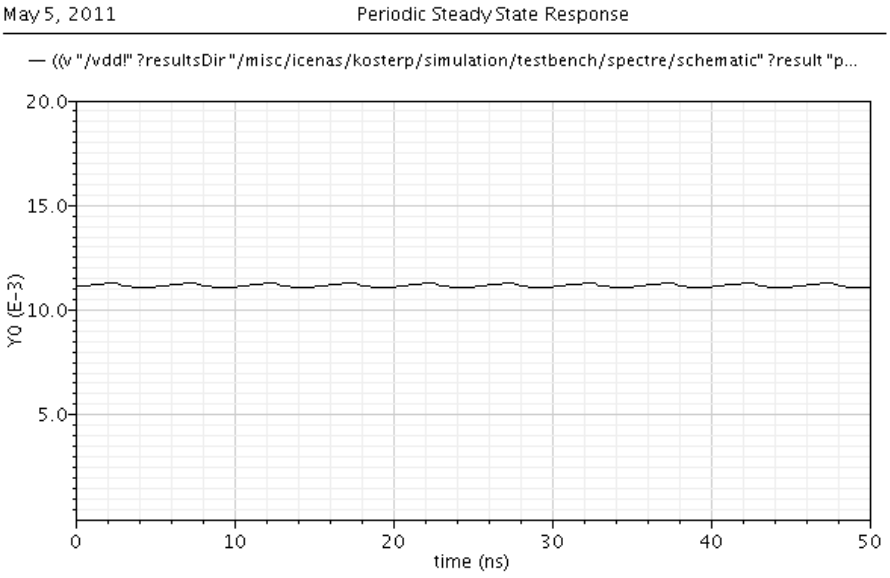

Figure 42: Power

	Desired	Obtained
IIP_3 [dBm]	*≥20*	*19.6*
EIRNV [nV/√Hz]	*≤3*	*2.9*
CL-gain [dB]	*≥12*	*11.9*
CL-BW [MHz]	*≥25*	*88.4*
Power [mW]	*≤10*	*11.2*

Table 13: Specifications verification

4.3 Summary:

In this chapter the basic amplifier topology proposed in chapter {2} is designed for high $IMFDR_3$ with the analysis results from chapter {3} considering some additional design considerations. From the clock frequency, closed-loop gain and resolution the minimum required UGF- and loopgain values were determined. These values then were respected during circuit- biasing and dimensioning considerationg regarding high $IMFDR_3$ design while additionally realizing slew-free- and stable circuit operation. Since the final results are close to desired no further tweaking is performed.

5 Conclusions and Recommendations:

*In this document an initial approach is given regarding the design of a high $IMFDR_3$ amplifier with proper mixer interfacing in CMOS 65nm technology. Conclusions that were drawn during the project developments are summarized in the following paragraph {**5.1**}. Like every project continuous efforts can be made to improve or extend on what was previously done. Suggestions for future work are therefore mentioned in the recommendations paragraph {**5.2**}.*

5.1 Conclusions:

Properties of the radio frequency (RF) environment like the presense of strong interferers and large signal propagation losses require high linearity and low noise radio front-ends (RFE) for small signal corruption. Both non-idealities are combined with defining the dynamic range (DR) parameter. The better the RFE is able to maintain the orginal signal (except for a scaling factor) the higher the DR is and the better varying signal levels can be processed. A well known parameter to specify the DR is the spurious-free dynamic range (SFDR). In this document however the third-order intermodulation-free dynamic range ($IMFDR_3$) parameter is used. With this parameter the lower end of the DR is determined by the noisefloor (F), rather than the sensitivity, for which additionally the minimum required signal-to-noise ratio (SNR_{min}) should be known.

Traditional RFE are believed to render a limited DR performance based upon the Friis theory of cascaded circuits, stating that both the noise and linearity of subsequent stages are downscaled by the gain of preceding stages. Hence a new RFE is envisioned in which a low noise mixer is directly connected to the antenna instead of using a low noise amplifier (LNA) first. The direct connection of the mixer to the antenna was already investigated giving significant results to proceed. Hence the current research request to design a high $IMFDR_3$ amplifier with proper mixer interfacing at the input (to compensate for the LNA gain loss) arrised. The circuit should be made in standard CMOS 65nm technology being the current design node.

Being familiar with the desire for a high linearity and low noise amplifier design a fully differential negative feedback amplifier is proposed. Negative feedback offers aside from high linearity many additional advantages like bandwidth- and terminal impedance modification while not effecting the noise. Fully differential operation further improves the linearity performance due to suppressing even-order distortion contributions and the noise performance due to less coupling. The average noise contribution nonetheless is doubled since the signal effectively encounters two- rather than one signal path. The linearity performance however remains the paramount design consideration and with the additional advantage of having doubled signal swings fully differential operation seems mandatory. Passive components are used to implement the amplifier feedback network since distortion isn't suppressed here. Although feedback resistors offer higher linearity performance in advance feedback capacitors are eventually chosen for offering more design freedom. To allow different Op Amp input- and output commen-mode voltages switched biasing is included within the capacitve feedback network. Consequently the amplifier operation will be discrete time which is allowed by the preceding discrete time mixer operation.

With the feedback network present high loopgain is demanded for high linearity performance. For this an Op Amp is used and allowed regarding the amplifier operation at intermediate frequencies. The Op Amp used is the folded cascode Miller Op Amp with common source output stage being referred to as the best solution for low IMD_3 in this particular case. Both Op Amp stages are additionally equipped with CMFB networks to have well defined common-mode voltages at the high impedance output nodes. Short circuit switches at the stages outputs are applied for preventing systematic offsets. The amplifier topology realized is referred to as a basic amplifier topology for high $IMFDR_3$ since large partions are still ideal or even omitting. Regarding the initial biasing and -dimensioning considerations for this circuit stable operation with voltage settling is aimed at and assured. Finally the functional- and performance testing gave sufficient results to proceed.

During the research the linearity- and noise dependencies upon the biasing and dimensioning are determined for final circuit design. The relative dimensioning of the feedback network has large influence upon the linearity, requiring maximum feedback factor for minimum closed-loop gain and hence small signal swings. The absolute dimensioning of the feedback network capacitors sizes should probably be maximized for less channel charge injection and smaller mismatch to increase the linearity. Regarding the Op Amp, the input stage shows large noise contribution and the output stage large distortion contribution demanding a low noise input stage- and a low distortion output stage design. The realization of a low noise input stage is completely determined by the biasing considerations. More particular the biasing of the signal- and current source MOSTs. For the signal MOSTs the transconductance should be maximized and for the current source MOSTs minimized. The signal MOSTs are influencing many design parameters limiting their strong use. The realization of a low distortion output stage is determined by biasing- and dimensioning considerations. The distortion is dominantly determined by the MOSTs output impedance and crossproducts of the transconductance and output impedance. The distortion can be reduced with low gate-source biasing and/or large MOST dimensioning.

To arrive at a final design for high $IMFDR_3$ a step design approach is followed. Starting with the clock frequency, closed-loop gain and resolution it is possible to determine the minimum required loopgain- and unity gain frequency. With additional considerations like slew free operation, stability and high $IMFDR_3$ biasing and dimensioning consideration are applied for the SC-FDA. Having determined the active component values this way the passives component values where determined by stability, voltage settling and gain requirements. The obtained amplifier performance specifications are an input-referred third-order intercept point (IIP_3) of 19.6dBm. An equivalent input-referred noise voltage (EIRNV) of 2.9nV/√Hz (at 20MHz). A closed-loop (CL) gain (A_{CL}) and CL bandwidth (BW_{CL}) of 11.9dB respectively 88.4MHz with a power consumption of 11.2mW. So the simulations resulted into performance specifications found in close agreement with desired.

5.2 Recommendations:

Considered a basic amplifier topology for high $IMFDR_3$ a first recommendation would be to update the existing SC-FDA topology. The feedback network implementation should result into reduced sensitivity to Op Amp gain for achieving the desired resolution. This additionally provides multi-phase operation in which switch timing can be used to create floating nodes for reducing channel charge injection effects, increasing the linearity. Additional to the feedback network realistic switches, biasing network and clock driver should be designed and the CMFB networks be provided with a means for performing frequency compensation.

The research results seem sufficiently adequate to propose biasing- and dimensioning considerations for high $IMFDR_3$ SC-FDA design in CMOS 65nm technology. From a scientific point of view the results lack an in dept understanding and can use an serious update.

Finally the circuit should be considered a multidimensional optimization problem for which the performance tradeoffs should be determined. When gained sufficient circuit understanding a more structured and elaborate design approach should be conducted for optimization.

A Abbreviations and Acronyms:

A Op Amp gain
A_1 input stage gain
A_2 output stage gain
a_0 offset voltage
a_1 linear gain
a_2 second-order nonlinear coefficient
a_3 third-order nonlinear coefficient
AB loopgain
A_{CL} closed-loop gain
ADC analog to digital converter
AMP amplifier

B feedback factor feedback network
BER bit error rate
bit binary digit
BW bandwidth
BW_{CL} closed-loop bandwidth

CL closed-loop

CM common-mode

CMFB common-mode feedback
CMOS complementary metal-oxide-semiconductor
CS common-source
CT continuous-time

DAC digital to analog converter
dB decibel
dB/dec decibel per decade
dBm decibel referred to milliwatt
dB/oct decibel per octave
dc direct current
DM differential-mode

DR dynamic range
DSP digital signal processing
DT discrete-time

EIRNV equivalent input-referred noise voltage
ESR equivalent series resistance

F noise floor
FDA fully differential amplifier
fF femto farad
F_{in} input referred noise floor
FC folded cascode
F_{clk} clock frequency

GBWP gain-bandwidth-product
gm tansconductance
Grad/sec giga radials per second

HDx x-order harmonic distortion

iac signal current
IC integrated circuit
ICD integrated circuit design
I_{DC} bias current
IF intermediate frequency
IIP_X x-order input-referred intercept point
IMD_X x-order intermodulation distortion
$IMFDR_X$ x-order intermodulation free dynamic range
ip peak relative current swing

kHz kilohertz
kΩ kilo-ohm

L length
LNA low noise amplifier
LPF low pass filter
LSB least significant bit

mA milliampère
maxacfreq maximum alternating current frequency
MHz megahertz
MIX mixer
MOST metal-oxide semiconductor transistor
mS milliSiemens
MSB maximum side-band

mV millivolt
mW milliwatt

nm nanometer
NMOST n-channel metal-oxide-semiconductor transistor
ns nanoseconds
nV/√Hz nanovolt per squart root of hertz

OL open-loop
Op Amp operational amplifier
OSR oversampling ratio
OSC oscillator

PAC periodic alternating current
pF picofarad
$\mathbf{P_{in\_min}}$ minimum input signal power
PMOST p-channel metal-oxide-semiconductor transistor
PNOISE periodic noise

PSS periodic steady-state

Q quality factor
Qc capacitor quality factor
QPSS quasi-periodic steady-state

R-CMFB resistive common-mode feedback
RF radio frequency
rms root-mean-square
RSB reference side-band
RX receiver

$\mathbf{s_1}$ sampling phase
$\mathbf{s_2}$ amplification phase
SC switched-capacitor
SCA switched-capacitor amplifier
SC-CMFB switched-capacitor common-mode feedback
SC-FDA switched-capacitor fully differential amplifier
S&H sample-and-hold
$\mathbf{SFDR_X}$ x-order spurious-free dynamic range
SNR signal-to-noise ratio
$\mathbf{SNR_{min}}$ minimum signal-to-noise ratio
specs. specifications
SR slew rate
std. standard

τ time constant
TD time domain

tech. technology

u input signal
uA microampère
UGF unity gain frequency
um micrometer

VCVS voltage controlled voltage source
V/Hz voltage per hertz
$\mathbf{V_{in}}$ input signal voltage
$\mathbf{V_{OUT}}$ output signal voltage

W width

WNL weakly nonlinear

y output signal

B SC-FDA Biasing:

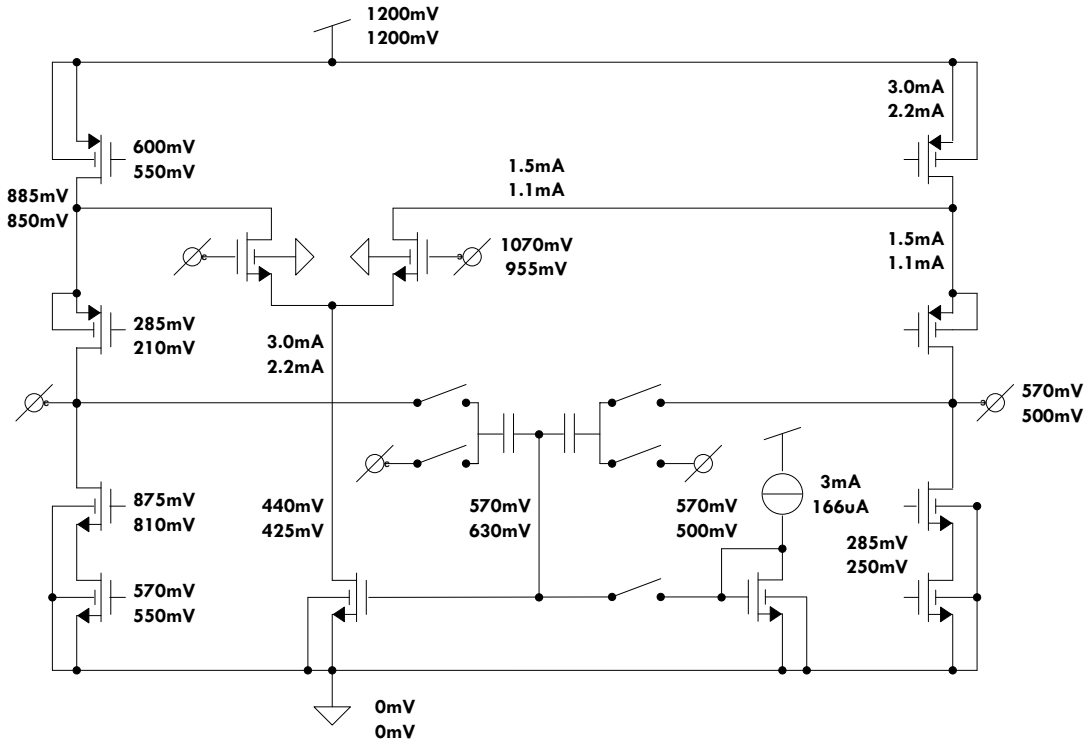

Figure 43: Input stage

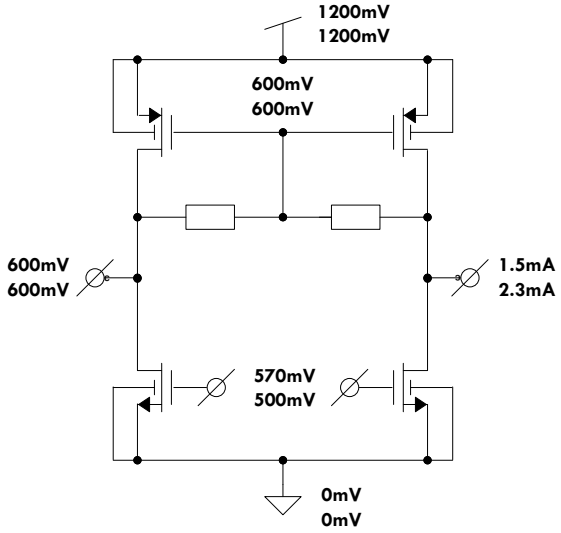

Figure 44: Output stage

C SC-FDA Dimensioning:

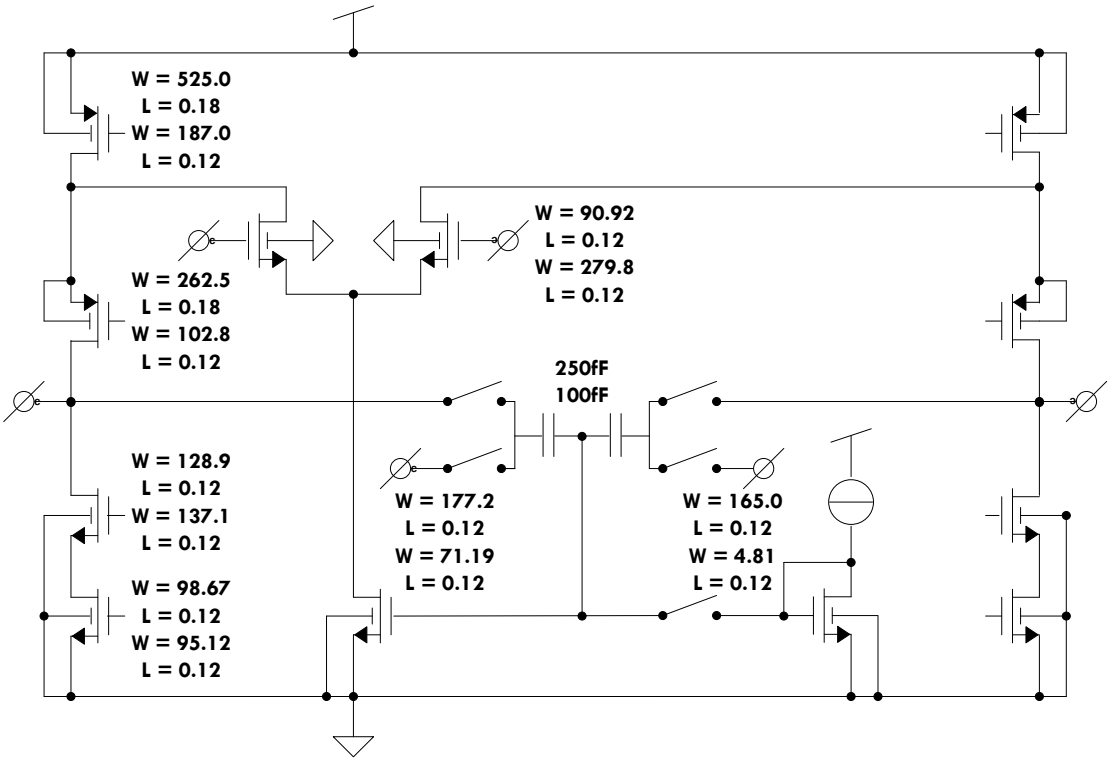

Figure 45: Input stage

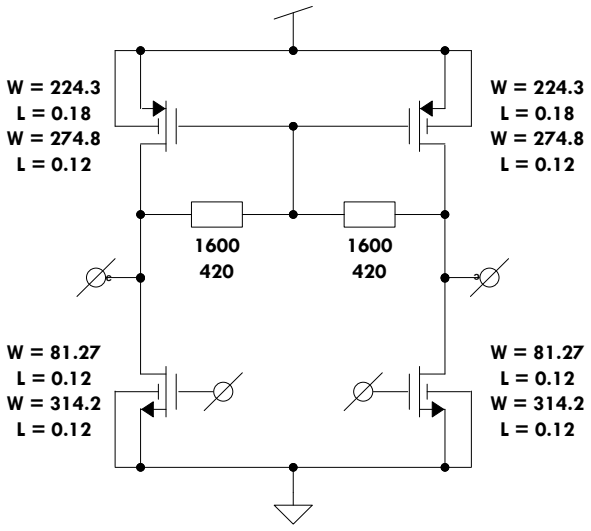

Figure 46: Output stage

Bibliography:

[1] B. Razavi, *"Design of Analog CMOS Integrated Circuits"*, Avenue of the Americas, NJ: McGraw-Hill, international edition, 2001, ISBN 0-07-118839-8.

[2] B. Razavi, *"RF microelectronics"*, Upper Saddle River, NJ: Prentice-Hall, 1998, ISBN 0-13-887571-5.

[3] T.S. Rappaport, *"Wireless Communications principles and practice"*, Upper Saddle River, NJ: Prentice-Hall, second edition, 2002, ISBN 0-13-042232-0.

[4] P. Wambacq and W. Sansen, *"Distortion Analysis of Analog Integrated Circuits"*, Dordrecht, The Netherlands: Kluwer Academic Publishers, 1998, ISBN 0-7923-8186-6.

[5] B. Hernes and T. Saether, *"Design Criteria for Low Distortion in Feedback Op Amp Circuits"*, Dordrecht, The Netherlands: Kluwer Academic Publishers, 2003, ISBN 1-4020-7356-9.

[6] M. Gustavsson, J.J. Wikner and N.N. Tan, *"CMOS Data Converters for Communications"*, Dordrecht, The Netherlands: Kluwer Academic Publishers, 2000, ISBN 978-1-4419-4968-4.

[7] M.C.M. Soer, *"Analysis and comparison of switch-based frequency converters"*, Enschede, The Netherlands: University of Twente, MSc Thesis, 2007.

[8] M.S. Oude Alink, *"Increasing the Spurious-Free Dynamic Range of an Integrated Spectrum Analyzer"*, Enschede, The Netherlands: University of Twente, MSc Thesis, 2008.

[9] W. Sansen, *"Distortion in Elementary Transistor Circuits"*, IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing, vol. 46, no. 3, March 1999.

[10] B. Hernes and W. Sansen, *"Distortion in Single-, Two- and Three-Stage Amplifiers"*, IEEE Transactions on Circuits and Systems – I: Regular Papers, vol. 52, no. 5, May 2005.

[11] K. Nagaraj, T.R. Viswanathan, K. Singhal and J. Vlach, *"Switched-Capacitor Circuits with Reduced Sensitivity to Amplifier Gain"*, IEEE Transactions on Circuits and Systems, vol. CAS-34, no. 5, May 1987.

[12] B. Carter, *"Fully Differential Op Amps Made Easy"*, Texas Instruments, Application Report, SLOA099, May 2002.

[13] R.G.H. Eschauzier and J.H. Huijsing, *"Frequency Compensation Techniques for Low-Power Operational Amplifiers"*, Dordrecht, The Netherlands: Kluwer Academic Publishers, fourth printing, 2002, ISBN 0-7923-9565-4.

[14] O. Choksi and L.R. Carley, *"Analysis of Switched-Capacitor Common-Mode Feedback Circuit"*, IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing, vol. 50, no. 12, December 2003.

[15] K.S. Kundert, *"A Test Bench for Differential Circuits"*, Designer's Guide Consulting, Inc. Version 1d, September 2006.

[16] K.S. Kundert, *"Simulating Switched-Capacitor Filters with SpectreRF"*, Designer's Guide Consulting, Inc. Version 6c, July 2006.

[17] Cadence Design Systems, Inc, *"Virtuoso® Spectre® Circuit Simulator Reference"*, Product Version 7.0.1, June 2008.